

關鍵字:

Ken Modified 07/21_**A00
Ken Modified 08/11_**A00
Ken Modified 08/13_**A00
Ken Modified 08/14_**A00
Ken Modified 08/17_**A00
Ken Modified 08/19_**A00

Blackwell-T4 8" Schematic
Cherry Trail - T4
2015-08-20
REV : A00

BOM 修改:

Snowfield : WU3701:054.03096.0001
Charger Mosfet (BOM變更)
Old P/N:ZZ.00215.037 Location: PU4603
New P/N: 84.03664.037 Location: PU4603
Second P/N:84.00920.037
TPS65982:65982074.65982.007Z ->074.65982.0B7Z
CPU:071.CHERY.0D0U->57VYD

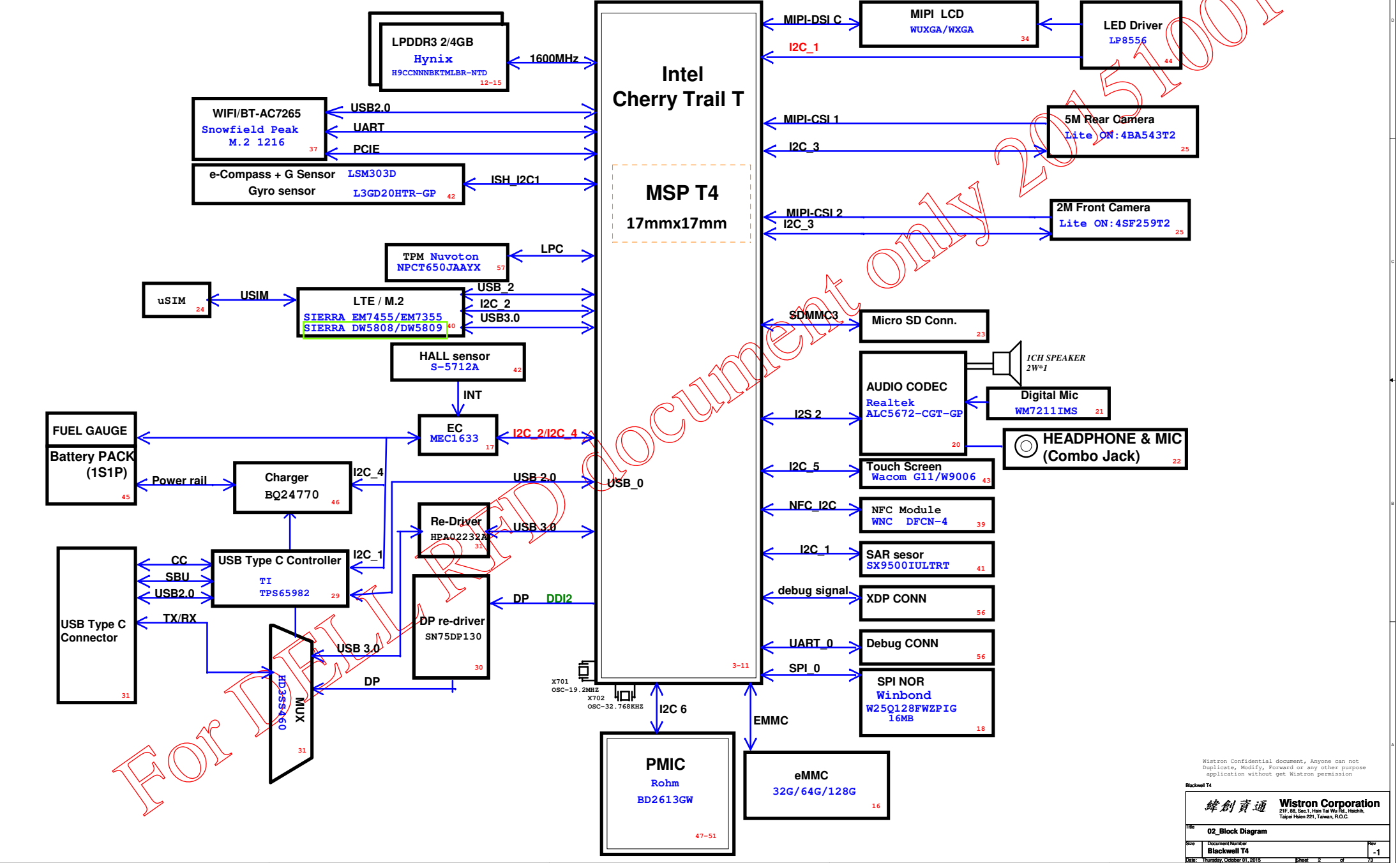
EC U1704 量產料號更改為:071.01633.0A0U
Cap 更改料號 78.10612.5BL->078.10612.05BN
Audio Codec U2001:071.03272.0003
Cancel XDPI,DB2,R735,R736,R740,R751
CAP更改料號 78.2R2B2.1SLRL -> 78.2R2B2.1SL
78.68034.1FLLL -> 78.68034.1FL

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<Core Design>

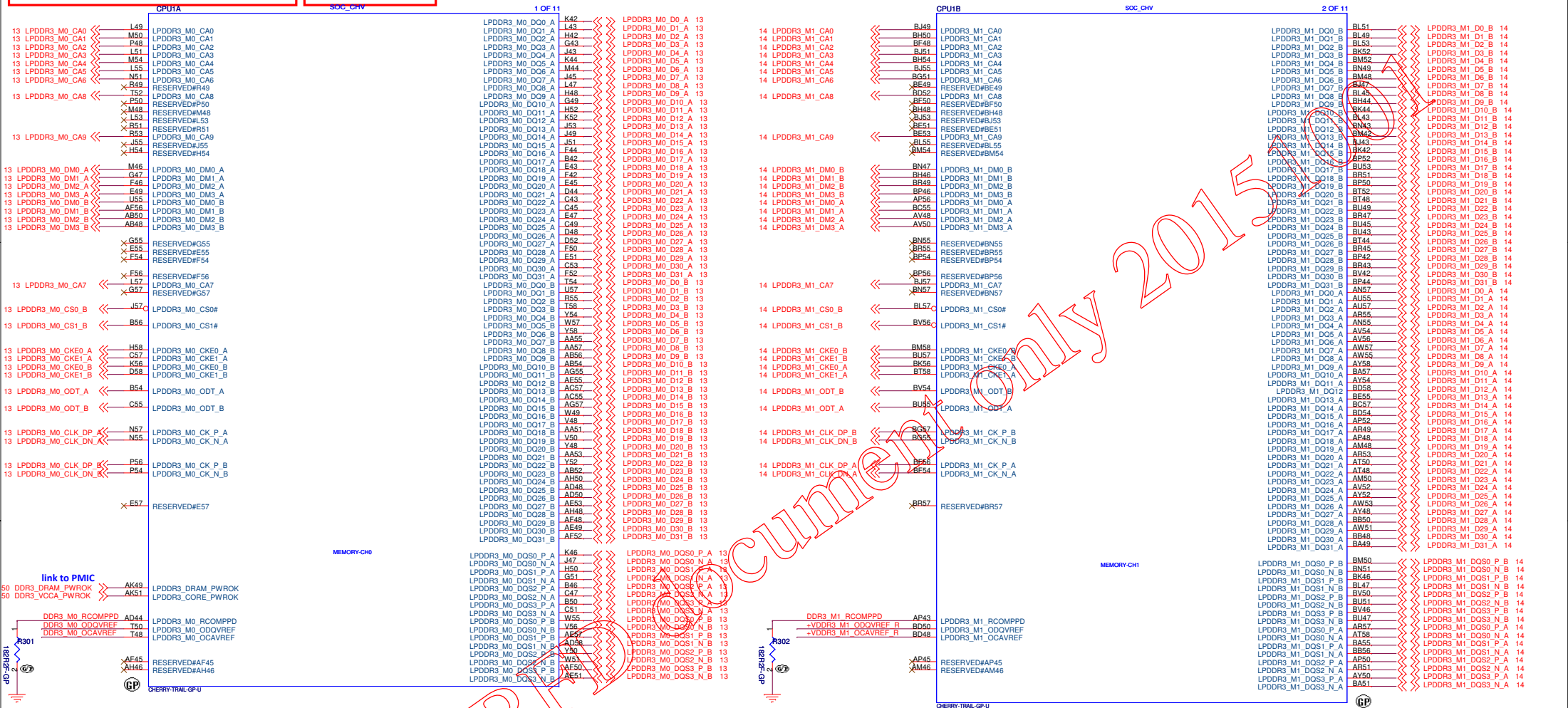
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title 01_Cover			
Size	Document Number		Rev
	Blackwell T4		-1
Date: Thursday, October 01, 2015		Sheet 1	of 73

Block Diagram



SOC MEM SECTION : 1&2

SSID=CPU



For layout: 3.3.1.1.2 LPDDR3 Bit and Byte Lane Swapping

- Data strobe swapping and data mask swapping **are not allowed**. For all memories, DM[n] must be mapped together with DQ Byte[n] and DQS/DQS#[n].
- Data bit swapping within a byte lane in the same channel is allowed, **except in the lowest two Bytes in each DRAM**. Swapping bits between bytes is not allowed.
- Byte lane swapping for LPDDR3 within same DRAM is allowed, **except the lowest two Bytes in each DRAM**. Byte swap between DRAM A and DRAM B is not recommended.
 - If swapping is used, DQ signals within a channel must match its associate DQS/ DQS# and DM signals.
 - In case customer has to do the Byte swap between DRAM A and DRAM B, ensure length matching for CLKA-CLKb is less than 20-mil.

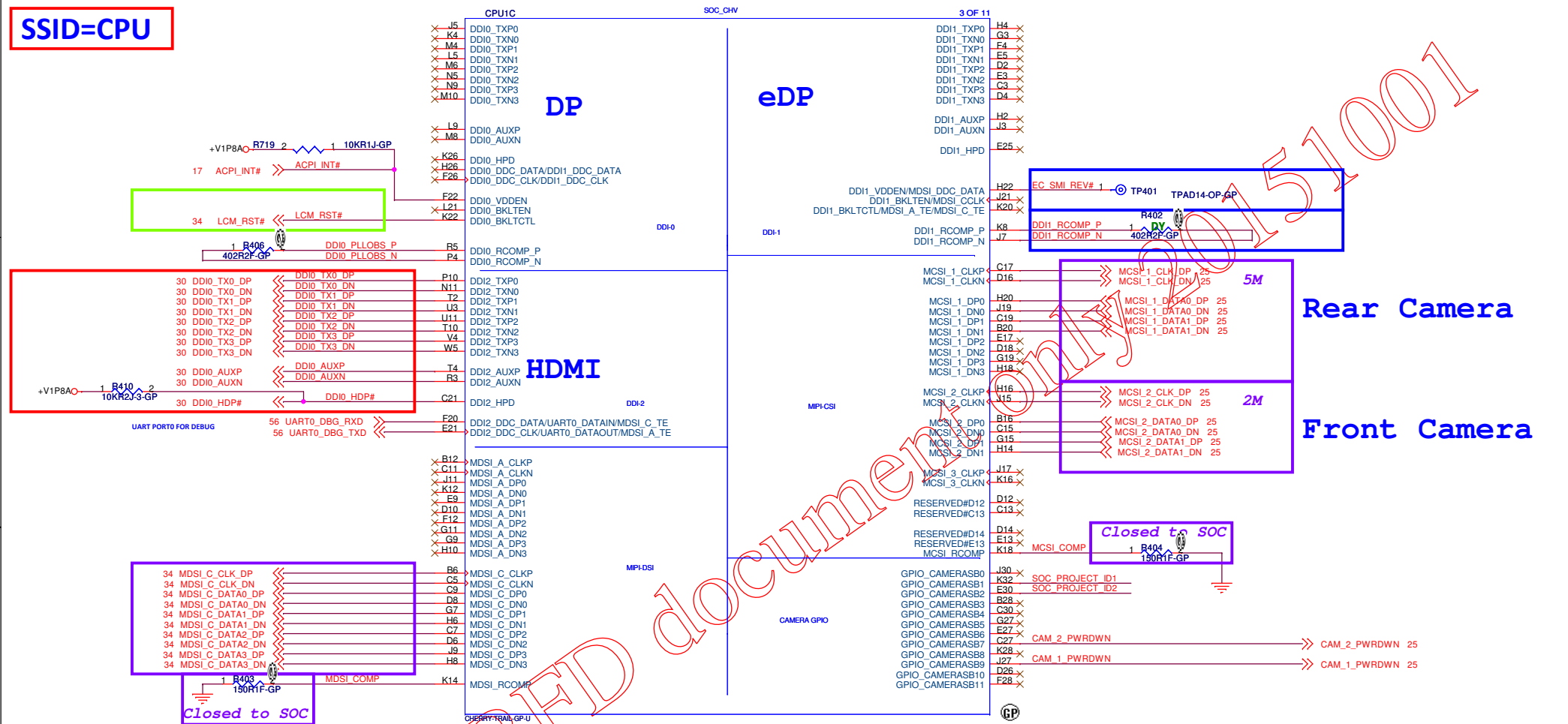
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Title	03_SOC (LPDDR3)
Size	Document Number
Rev	-1
Date	Thursday, October 01, 2015
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SOC : DDI 0&1 / MIPI-DIS/MIPI-CSI/MIPI-GPIO

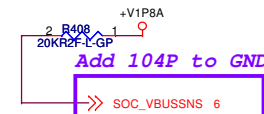
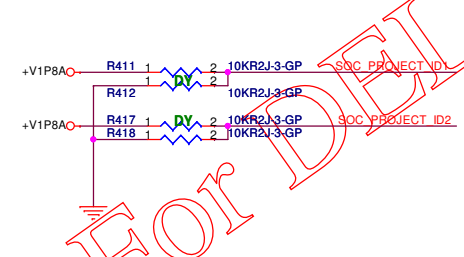
SSID=CPU



SOC_PROJECT ID

PROJECT	PROJECT_ID2	PROJECT_ID1
Blackwell-T3	0	0
Blackwell-T4	0	1
Somerset-T3	1	0
Somerset-T4	1	1

PROJECT ID



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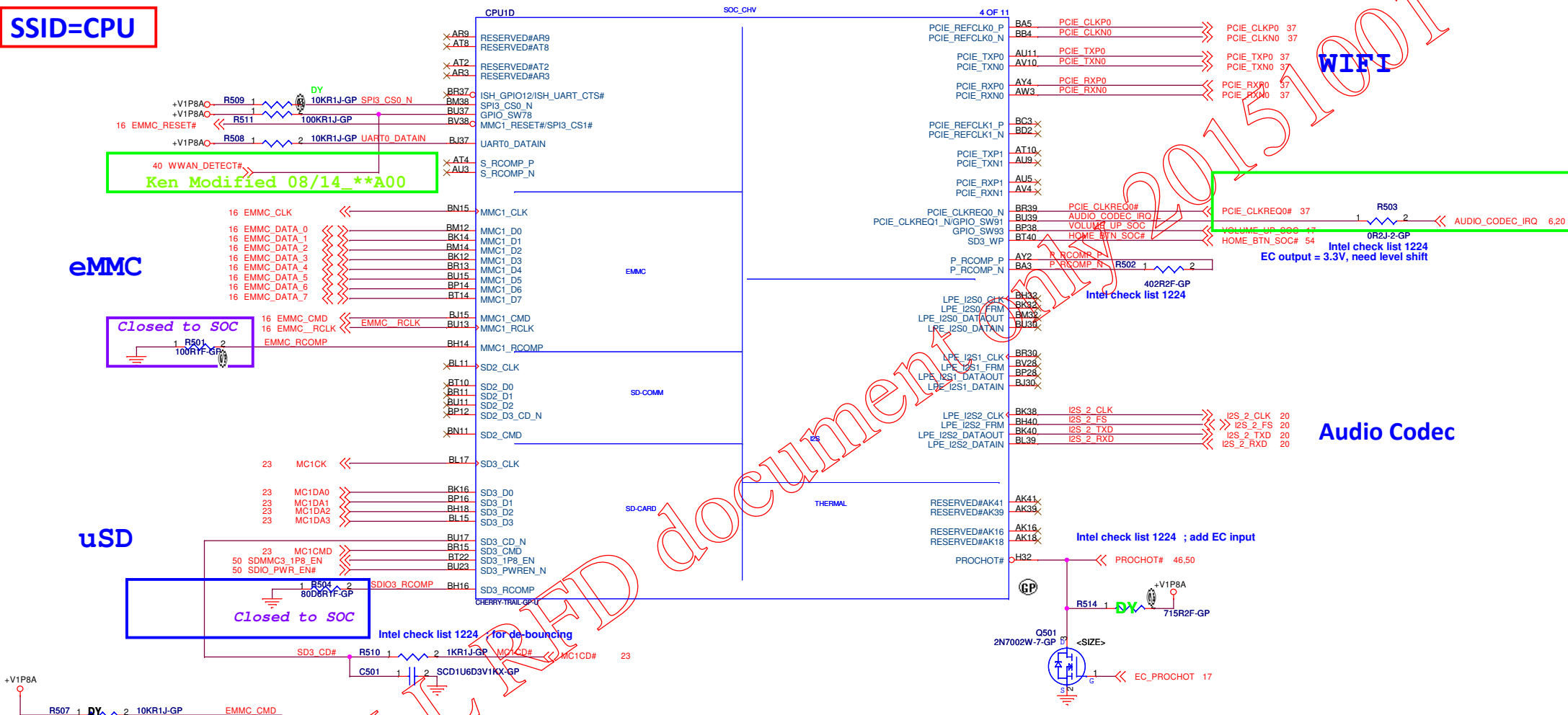
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Title	04_SOC (eDP/HDMI/MIPI)	
Size	Document Number	Rev
	Blackwell T4	-1
Date:	Thursday, October 01, 2015	Sheet 4 of 73

SOC : eMMC/SD/GPIO/I2S

SSID=CPU

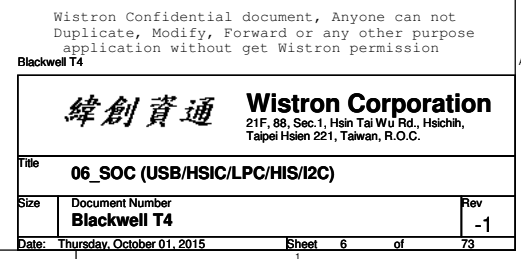


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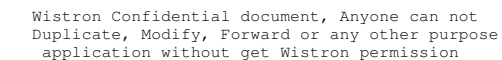
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title 05_SOC (EMMC/SD/GPIO/I2S)	
Size Document Number	Rev -1
Date: Thursday, October 01, 2015	Sheet 5 of 73

SSID=CPU



SSID=CPU

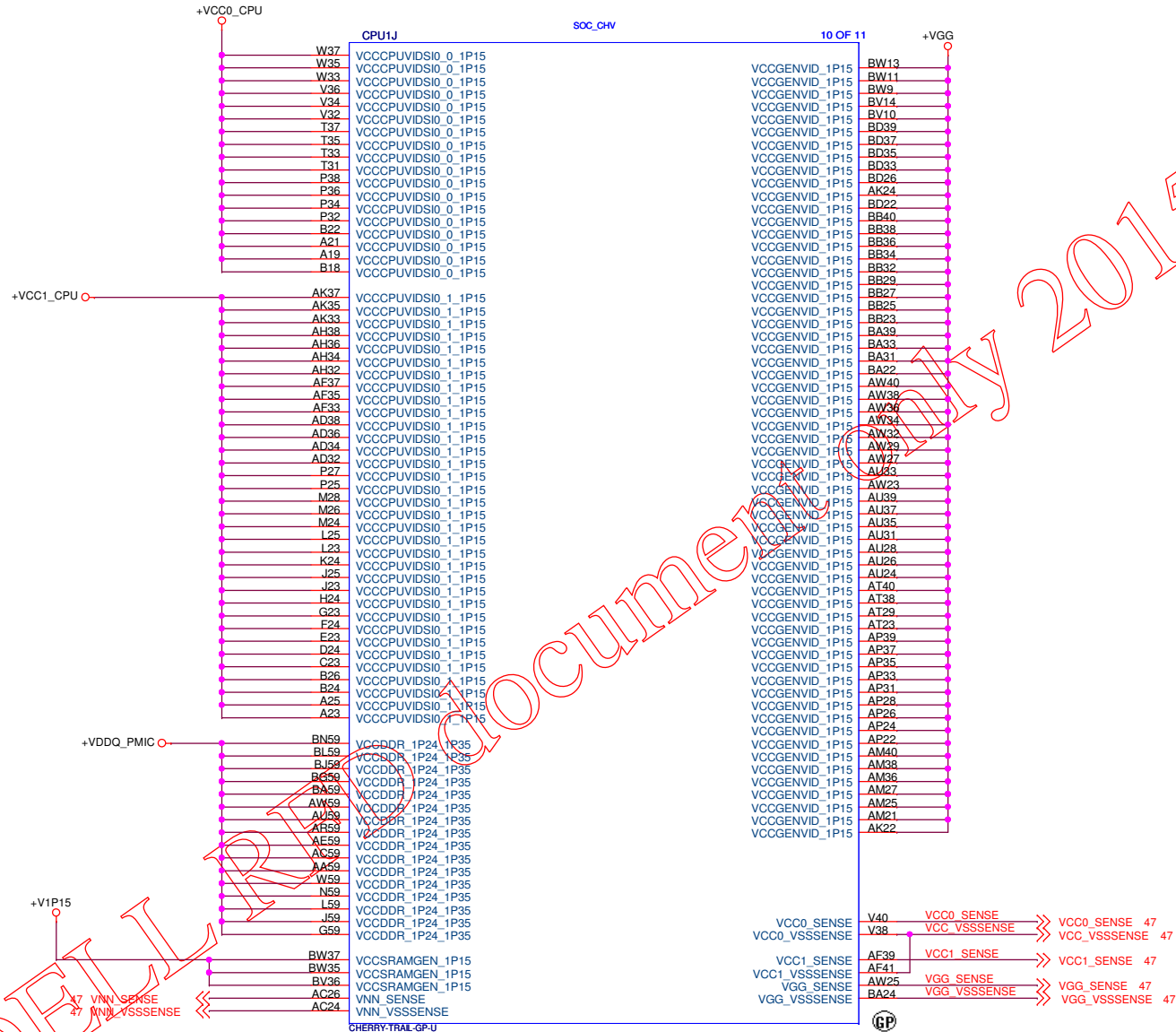


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Size	Document Number Blackwell T4	Rev -1
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SOC : VCC/VNN

SSID=CPU



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Title

09_SOC (VCC/VNN)

Size

Document Number

Blackwell T4

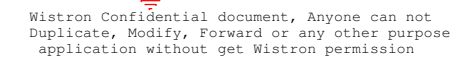
Rev

-1

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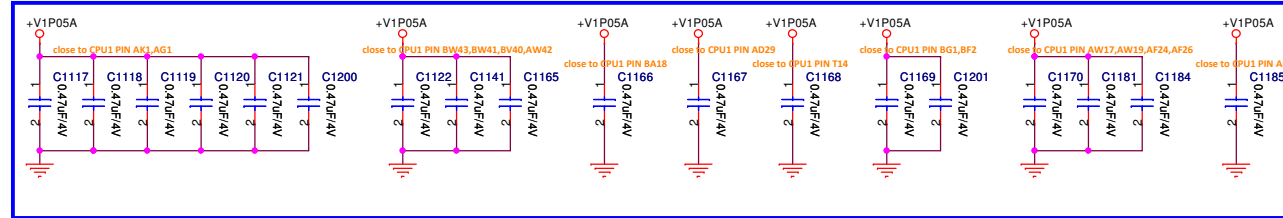
SSID=CPU



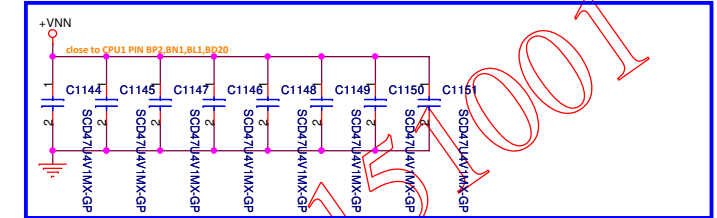
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Size	Document Number Blackwell T4	Rev -1
Date:	Thursday, October 01, 2015	Sheet 10 of 73

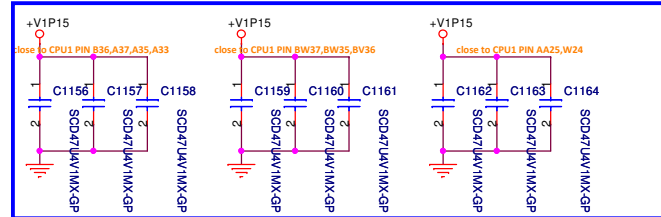
+V1P05A



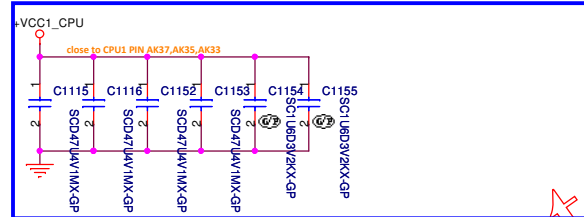
+VNN



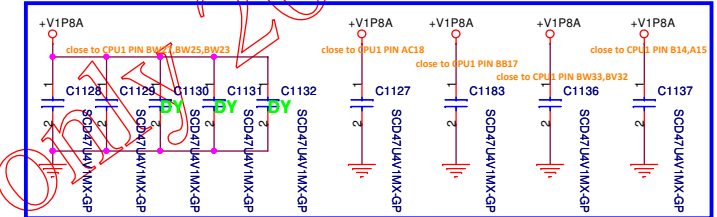
+V1P15



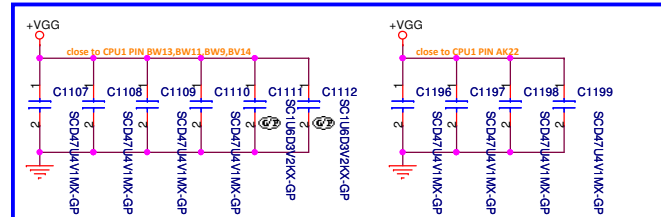
+VCC1_CPU



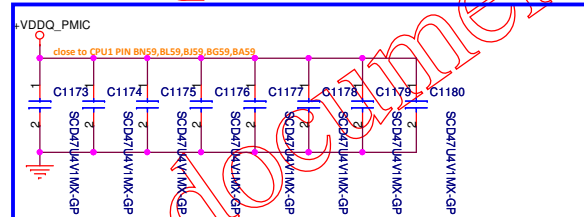
+V1P8A



+VGG



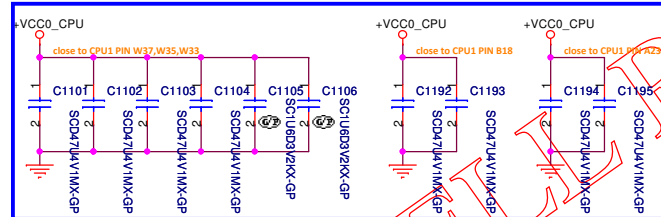
+VDDQ_PMIC



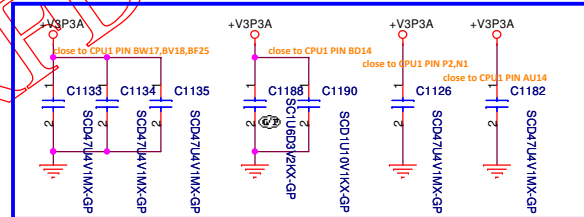
+V1P2A



+VCC0_CPU



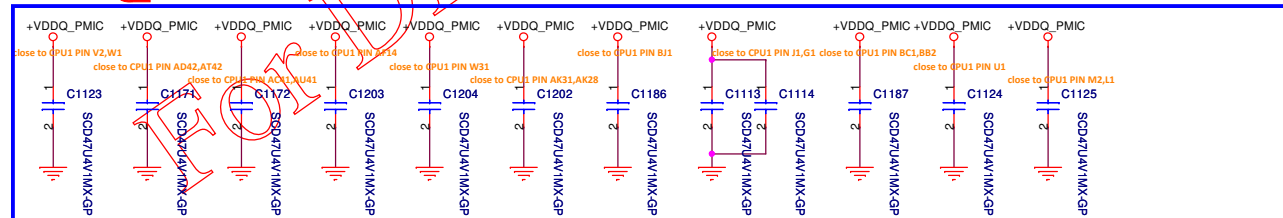
+V3P3A



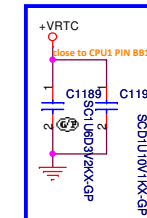
+VSDIO



+VDDQ_PMIC



+VRTC



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Title 11_CPU (VLV2 Decoupling)

Size Document Number Blackwell T4 Rev -1

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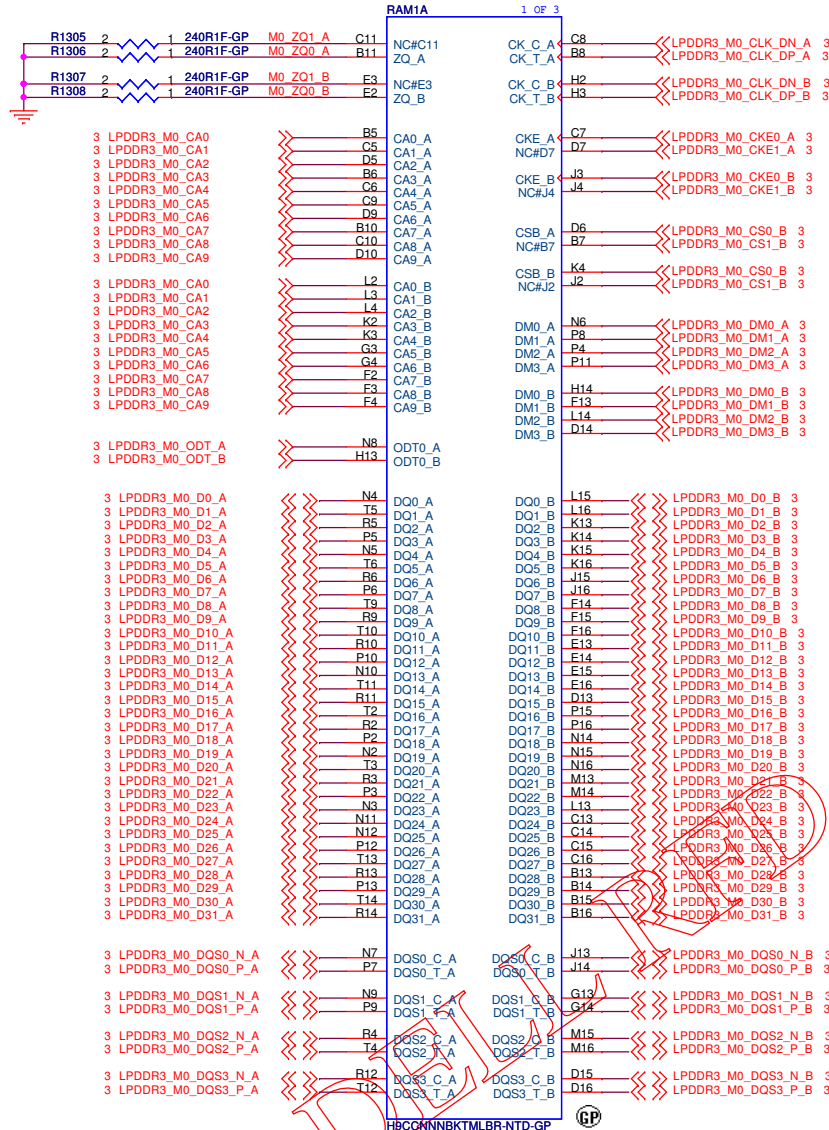
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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.					
Title 12_LPDDR3 (Reserved)					
Size	Document Number Blackwell T4				Rev -1
Date: Thursday, October 01, 2015			Sheet 12	of	73

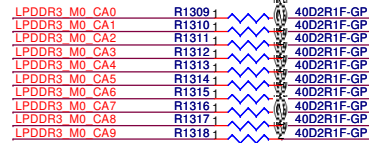
LPDDR3 MEMORY CHANNEL A

SSID=MEMORY

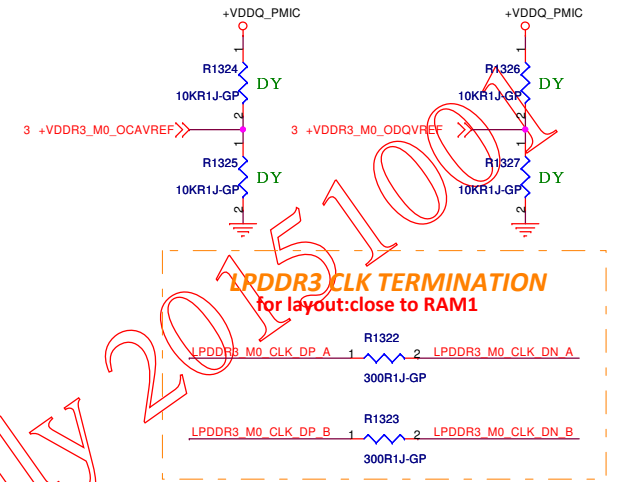
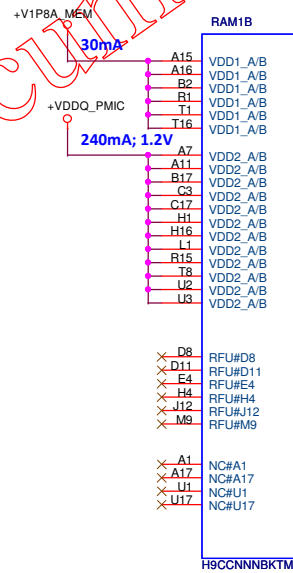
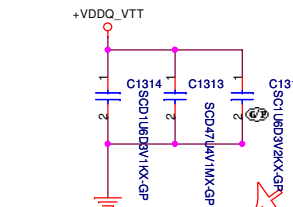
H9CCNNN8KTMBR-NTM-GP



for layout:
colsed to RAM1



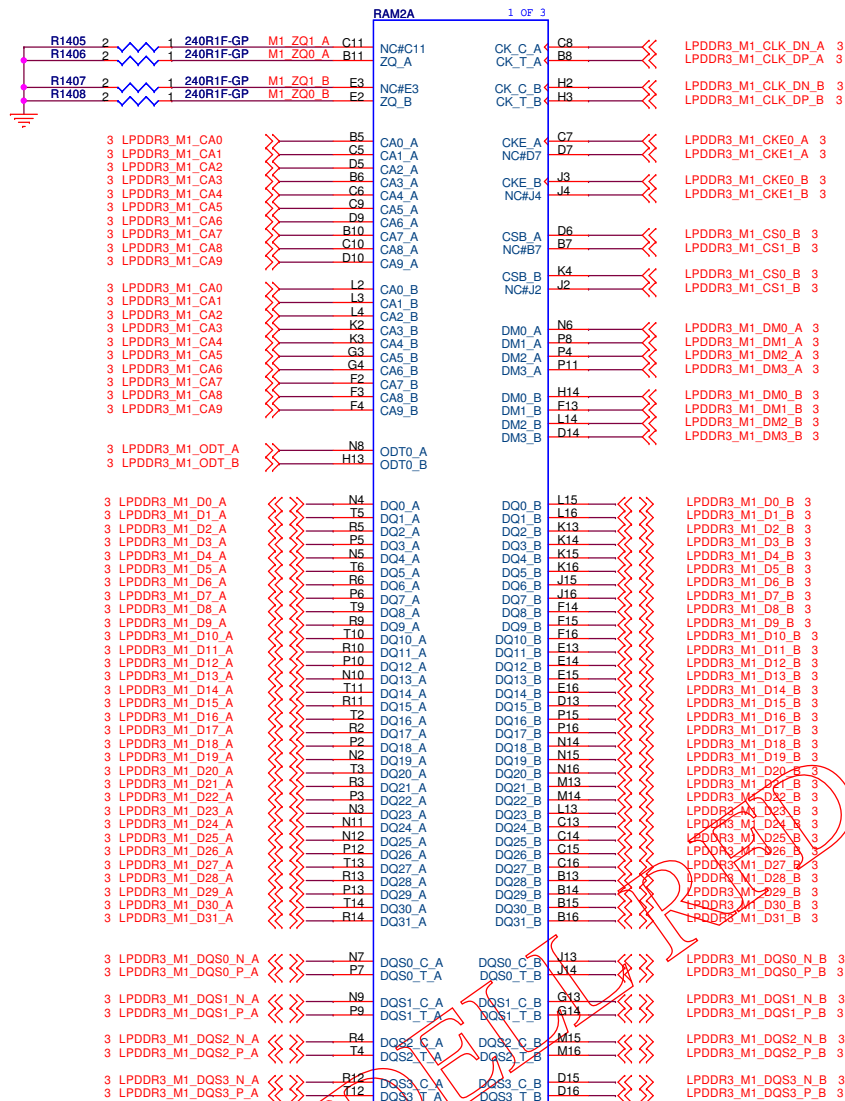
LPDDR3 CA TERMINATION



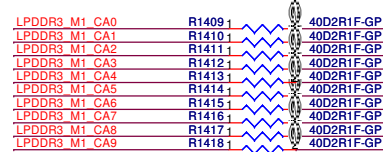
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LPDDR3 MEMORY CHANNEL B SSID=MEMORY

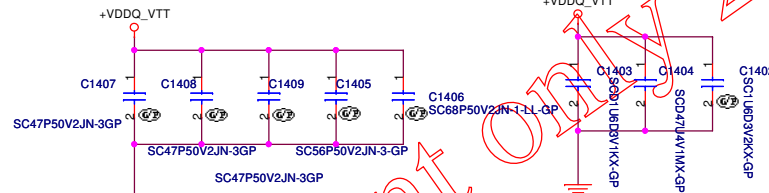
H9CCNNN8KTMBR-NTM-GP



for layout:
close to RAM2

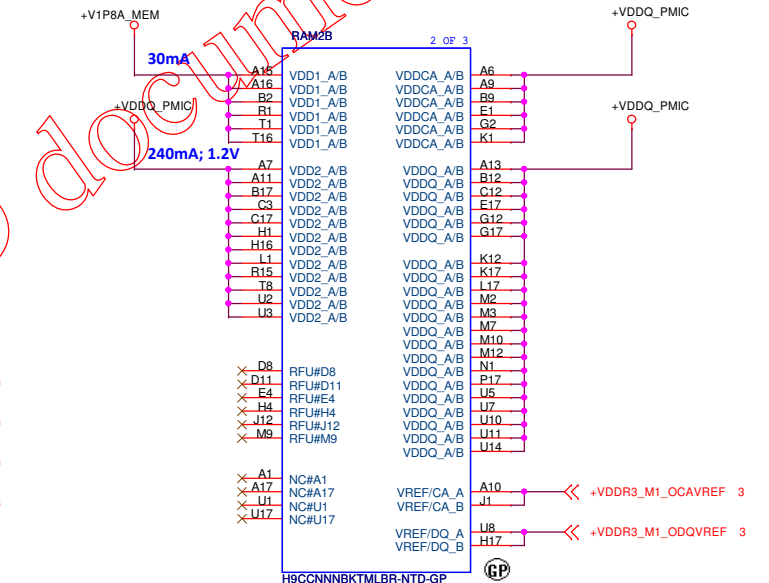
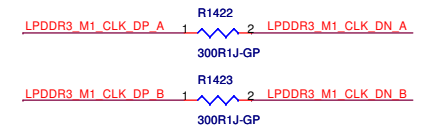


LPDDR3 CA TERMINATION



LPDDR3 CLK TERMINATION

for layout: close to RAM2



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Title 14_LPDDR3_RAM2(H9CCNNN8KTMBR)

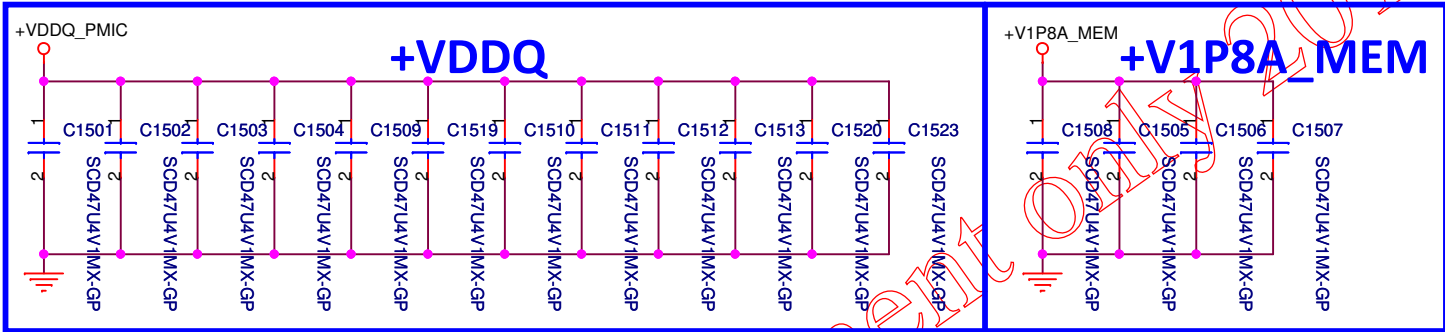
Size Document Number Blackwell T4 Rev -1

Date: Thursday, October 01, 2015 Sheet 14 of 73

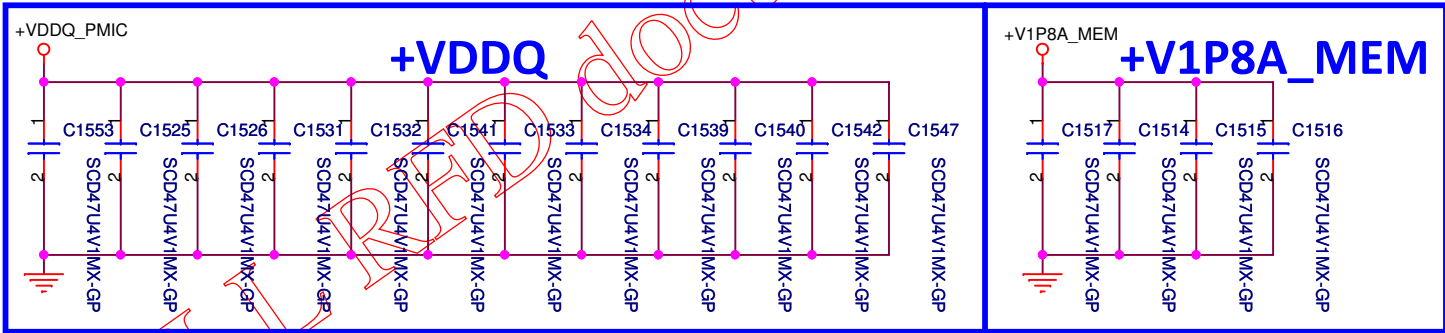
LPDDR3 DECOUPLING CAPACITORS

SSID=MEMORY

LPDDR3 MEMORY CHANNEL A



LPDDR3 MEMORY CHANNEL B



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Title15_LPDDR3_TERMINATIONS		
Size	Document NumberBlackwell T4	Rev-1
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SSID=EMMC

TPAD14-OP-GP	TP1601	1	EMMC_CMD
TPAD14-OP-GP	TP1602	1	EMMC_RESET#

Pin connection diagram for the EMMC1A interface. The diagram shows connections for 1 of 2 pins. On the left, pins C6, VDD, N4, P3, P5, VDD, F5, VDDF, J10, K9, VDDF, C2, VDDI, M5, M6, CLK, K5, RST#, H5, and DATA_STROBE are listed. On the right, pins A3 through A6, B2 through B6, and C4 through C6 are listed. The connections are as follows: C6 to VDD, N4 to VDD, P3 to VDD, P5 to VDD, F5 to VDDF, J10 to VDDF, K9 to VDDF, C2 to VDDI, M5 to CMD, M6 to CLK, K5 to RST#, H5 to DATA_STROBE, A3 to EMMC DATA 0, A4 to EMMC DATA 1, A5 to EMMC DATA 2, A6 to EMMC DATA 3, B2 to EMMC DATA 4, B3 to EMMC DATA 5, B4 to EMMC DATA 6, B5 to EMMC DATA 7, C4 to VSS, C5 to VSS, C6 to VSS, G5 to VSS, H10 to VSS, J5 to VSS, K8 to VSS, N2 to VSS, N9 to VSS, P4 to VSS, and P6 to VSS. A large red watermark '2012' is overlaid on the diagram.

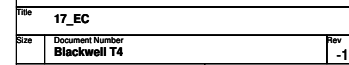
The diagram illustrates the eMMC interface between the Valleyview-T SoC and the eMMC Device0. The Valleyview-T SoC is represented by a light blue box containing a green 'CORE' block and an orange 'DRIVER' block. The 'DRIVER' block is connected to a 'V1p8s' supply and a '49.9 Ohms' resistor leading to ground. The 'eMMC Device0' is shown as a light blue box containing a yellow 'Core' block and a blue 'I/O' block. The 'I/O' block is connected to 'VEMMC1' and 'VEMMC2' supplies. The interface signals are as follows:

- EMMC_0_CLK**: A single arrow pointing from the Valleyview-T DRIVER to the eMMC Device0 I/O block.
- EMMC_0_D[7:0]**: A bidirectional arrow between the Valleyview-T DRIVER and the eMMC Device0 I/O block.
- EMMC_0_CMD**: A single arrow pointing from the Valleyview-T DRIVER to the eMMC Device0 I/O block.
- EMMC_0_RST_N**: A single arrow pointing from the Valleyview-T DRIVER to the eMMC Device0 I/O block.

Power and ground connections are also shown:

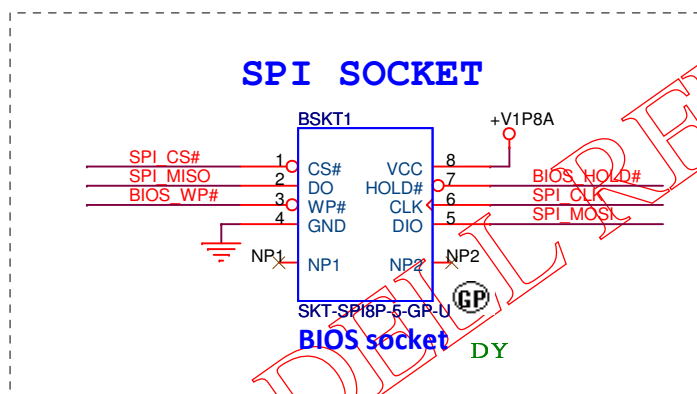
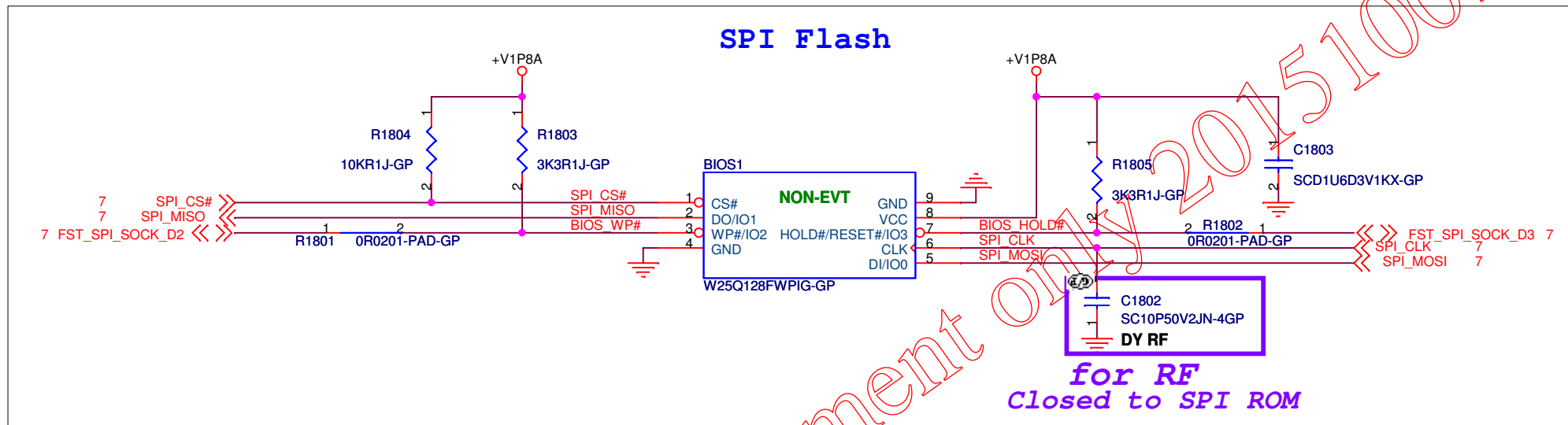
- VNN**: Connected to the Valleyview-T CORE.
- V1p8s**: Connected to the Valleyview-T DRIVER.
- VEMMC1** and **VEMMC2**: Connected to the eMMC Device0 Core.
- 49.9 Ohms**: A resistor connected between the Valleyview-T DRIVER and ground.

Rev	-1
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SPI ROM SSID=Flash.ROM

Need to made FPC for new debug port.



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Title

18_SPI NOR

Size

Document Number
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-1

Date: Thursday, October 01, 2015

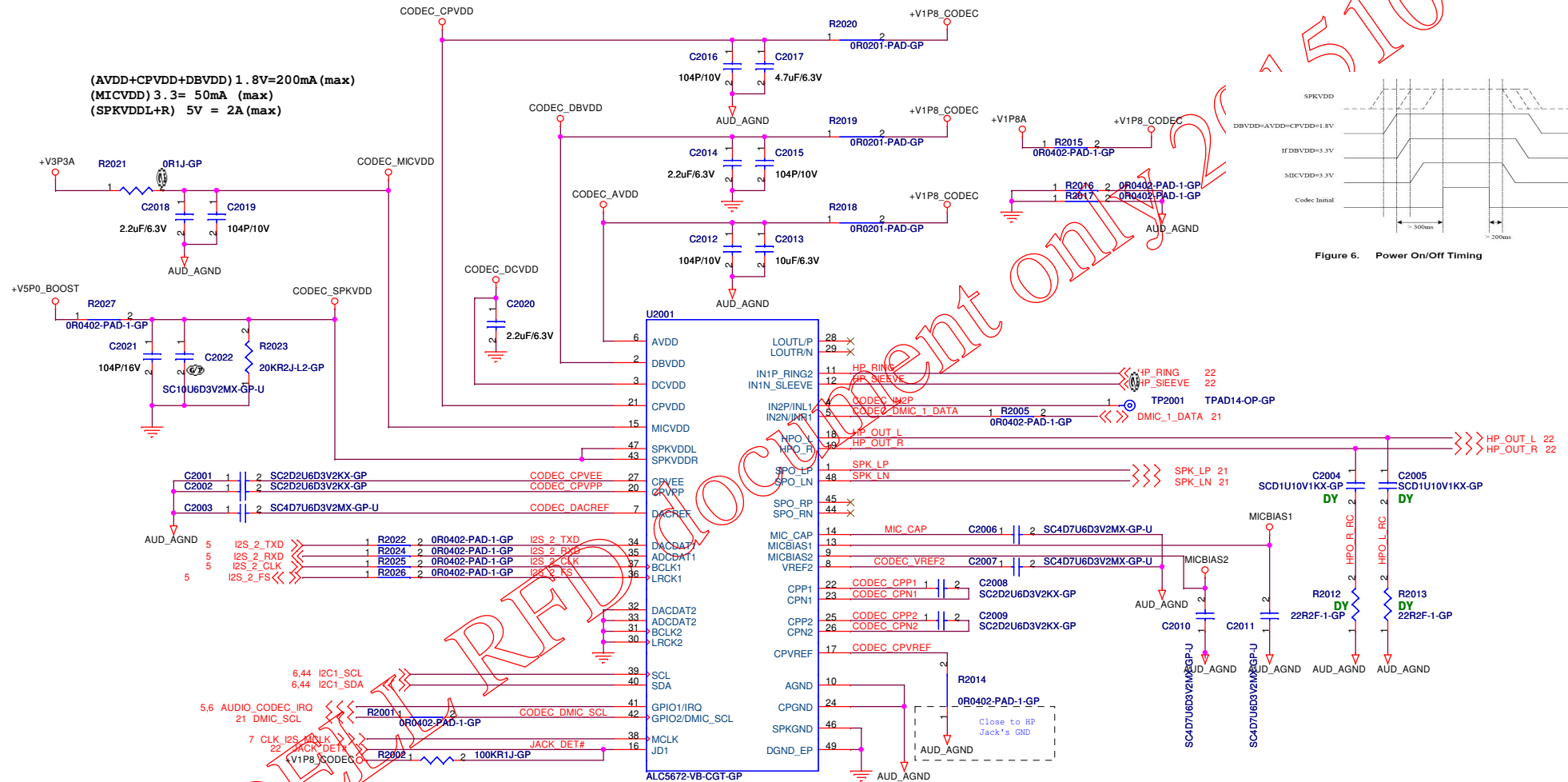
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Title 19_Thermal Protect(Reserved)		
Size	Document Number	Rev
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Title **20_AUDIO CODEC**

Size Document Number

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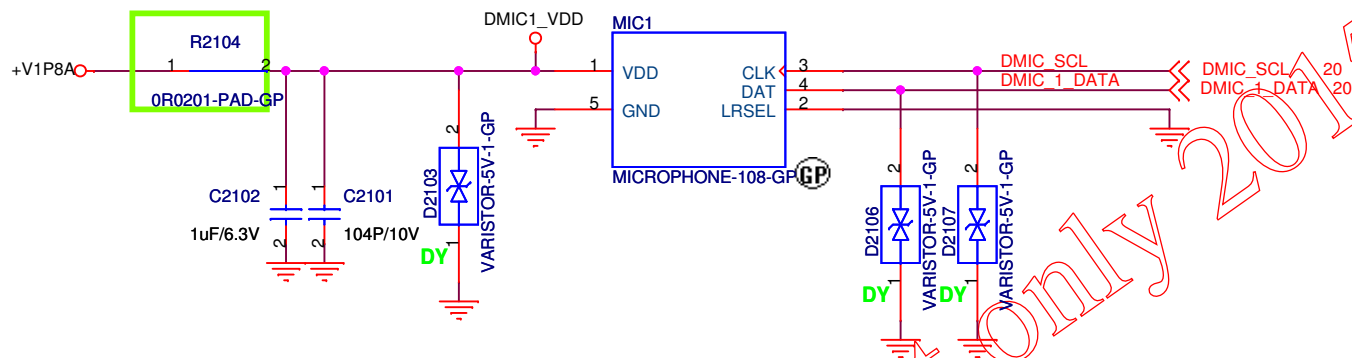
Rev

-1

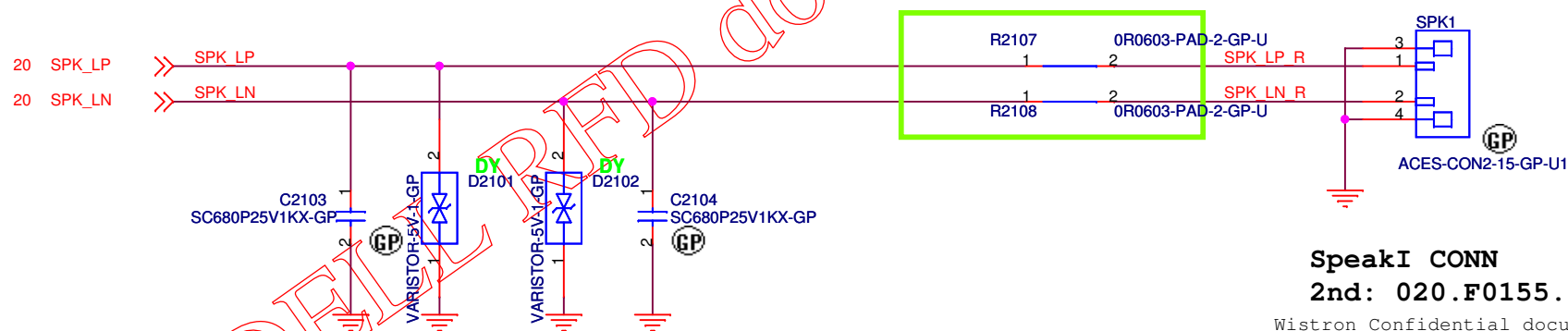
DMIC

SSID=AUDIO

need to check DMIC position and SEL pin define



SPEAKER



SpeakI CONN

2nd: 020.F0155.0004

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<Core Design>

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Title 21_AUDIO AMP/DMIC/SPK

Size Document Number
Blackwell T4

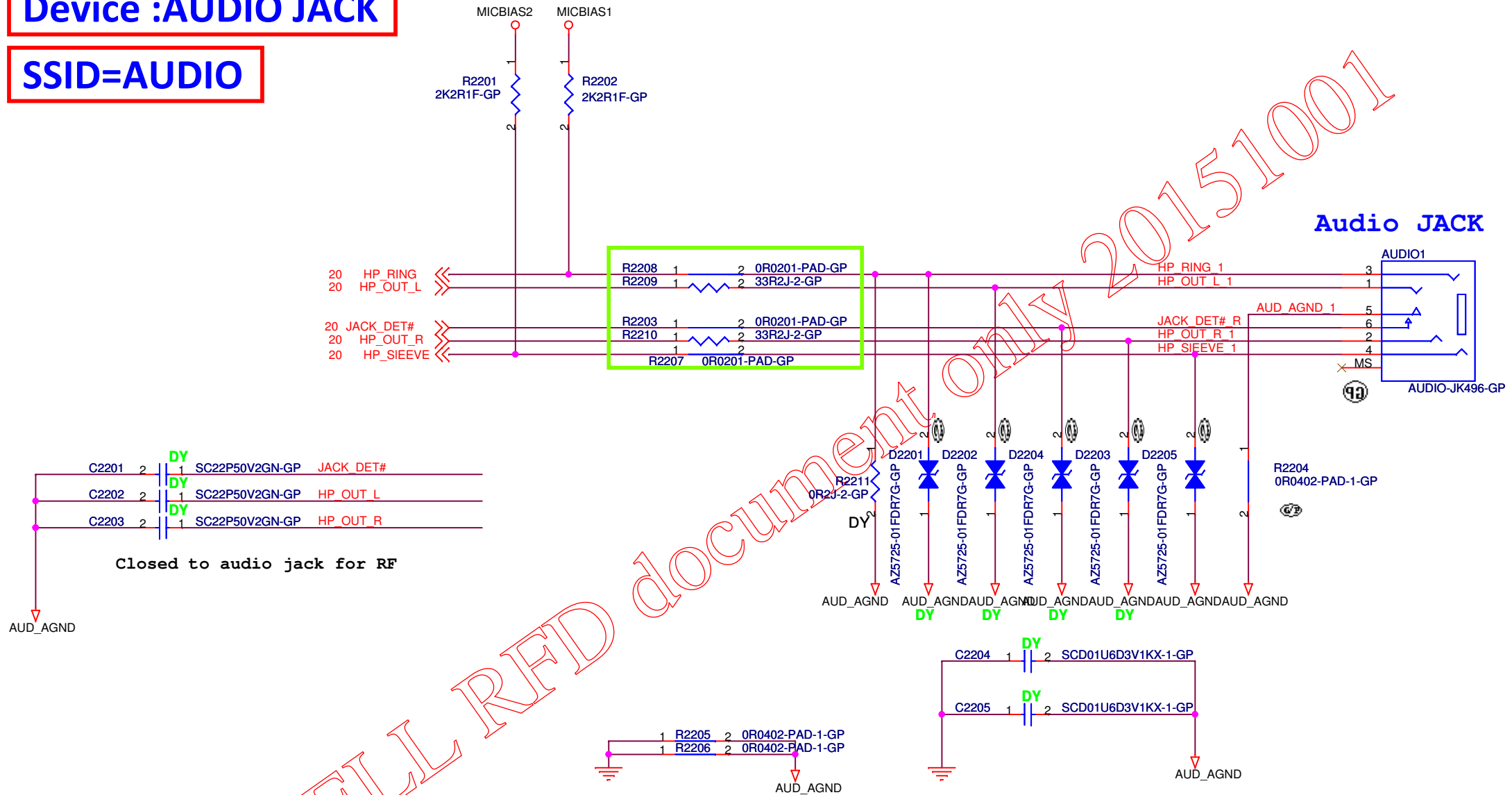
Rev
-1

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Device :AUDIO JACK

SSID=AUDIO



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Title
22_Audio JACK

Size
Document Number
Blackwell T4

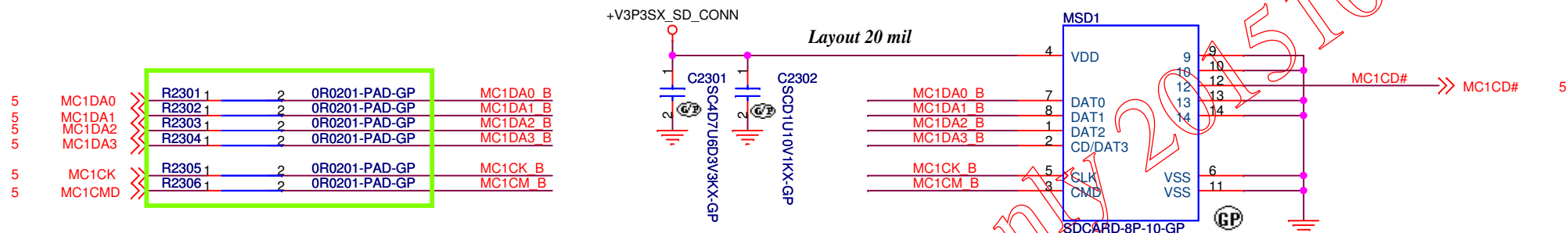
Rev
-1

Date: Thursday, October 01, 2015

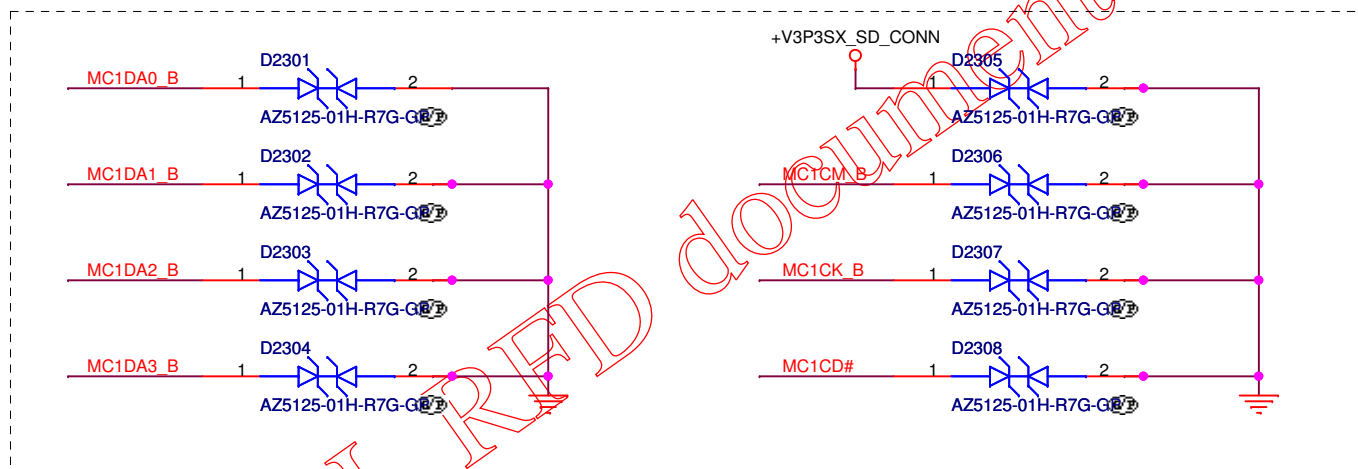
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SD CARD

SSID=SDIO



for ESD/RF Closed to SDC1



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Title 23_uSD Card CONN

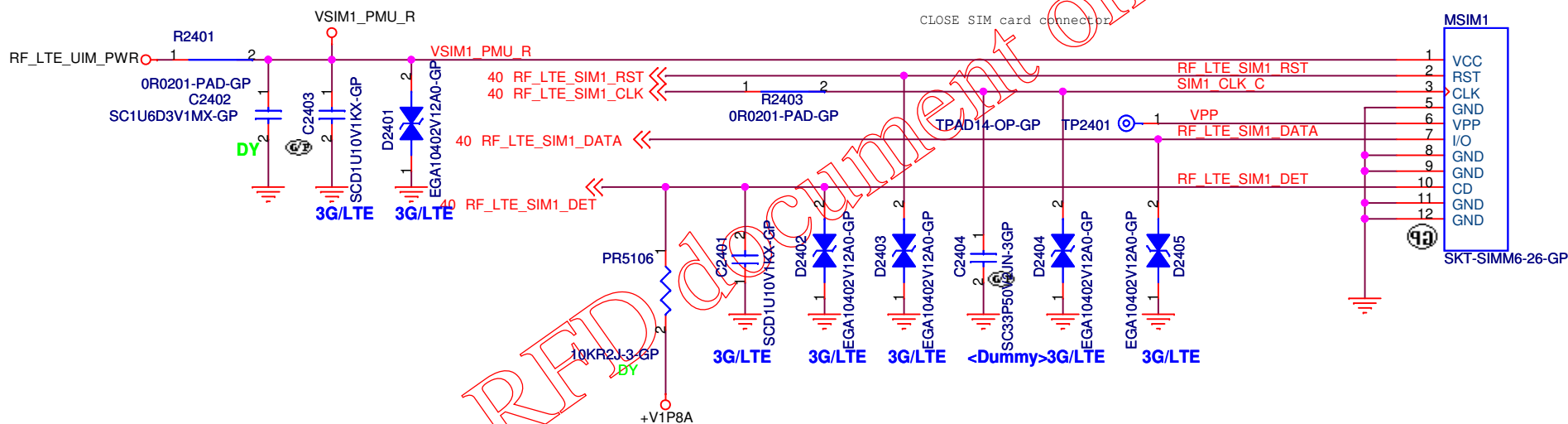
Size Document Number Blackwell T4

Rev -1

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SIM CARD

SSID=Wireless



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Title 24_uSIM CONN

Size Document Number Blackwell T4

Rev -1

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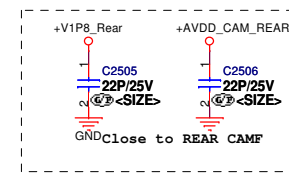
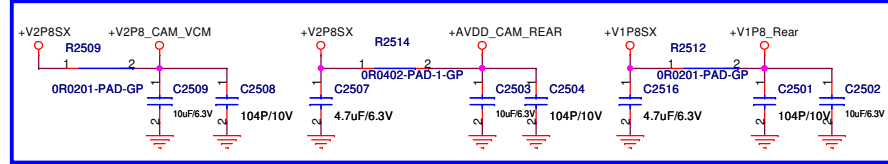
Rear Camera

5M Rear Camera

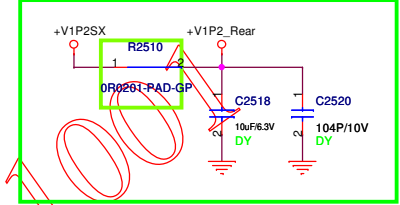
Lite ON:4BA543T2

SSID=CAMERA

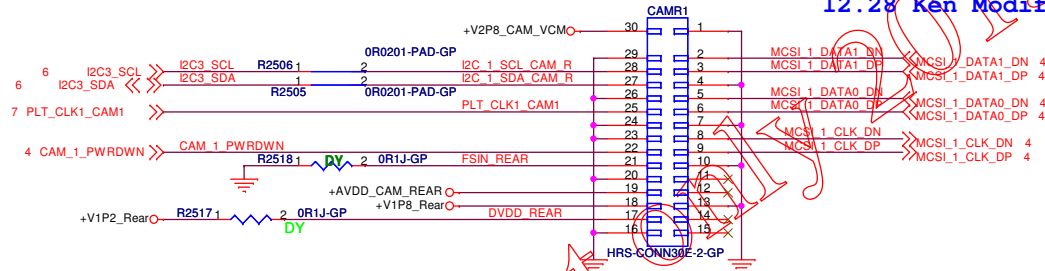
Rear Camera Power



Cammera Team Check List -12.26



12.28 Ken Modified



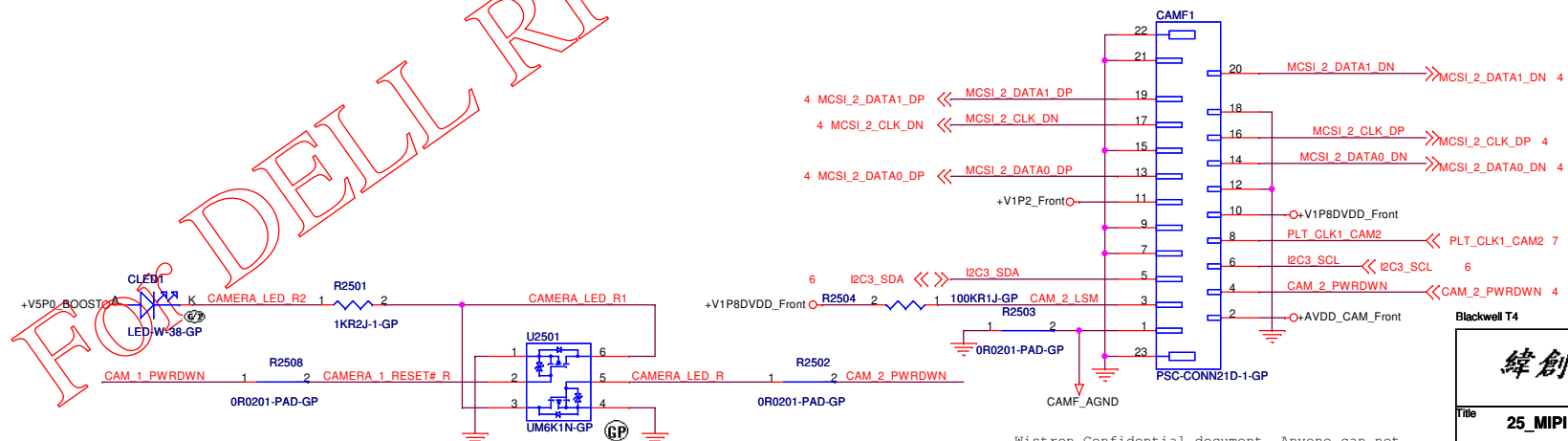
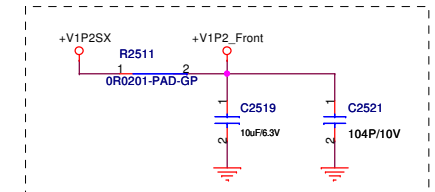
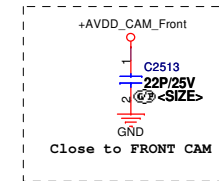
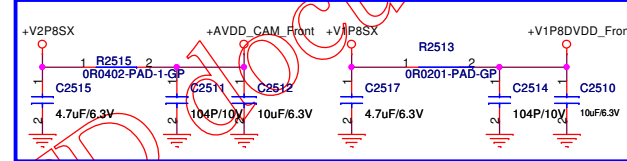
Front Camera

2M Front Camera

Lite ON:4SF259T2

need to check the connector & pin define

Front Camera Power



Blackwell T4

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Title			25_MIPI CAMERA CONN
Size	Document Number	Rev	
	Blackwell T4	-1	
Date:	Thursday, October 01, 2015	Sheet	25 of 73

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Title26_Camera_3D		
Size	Document NumberBlackwell T4	Rev-1
Date: Thursday, October 01, 2015		Sheet 26 of 73

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Title

27_USBPHY/SW(Reserved)

Size

Document Number

Blackwell T4

Rev

-1

Date: Thursday, October 01, 2015

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Reserved

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Title

28_Full/MICRO USB CONN(Reserved)

Size

Document Number

Blackwell T4

Rev

-1

Date: Thursday, October 01, 2015

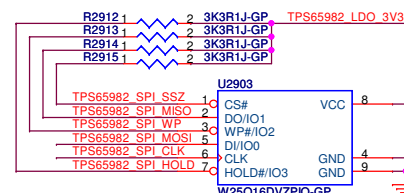
Sheet 28 of 73

SSID=USB

LEVEL SHIFT

6 CPU_USB_OC# << CPU_USB_OC# D2901 A K DB2U31600L-GP TPS65982 GPIO8

FLASH



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Title	29 USB TYPE C 1
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Size	Document Number Blackwell T4
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Date: Thursday, October 01, 2015

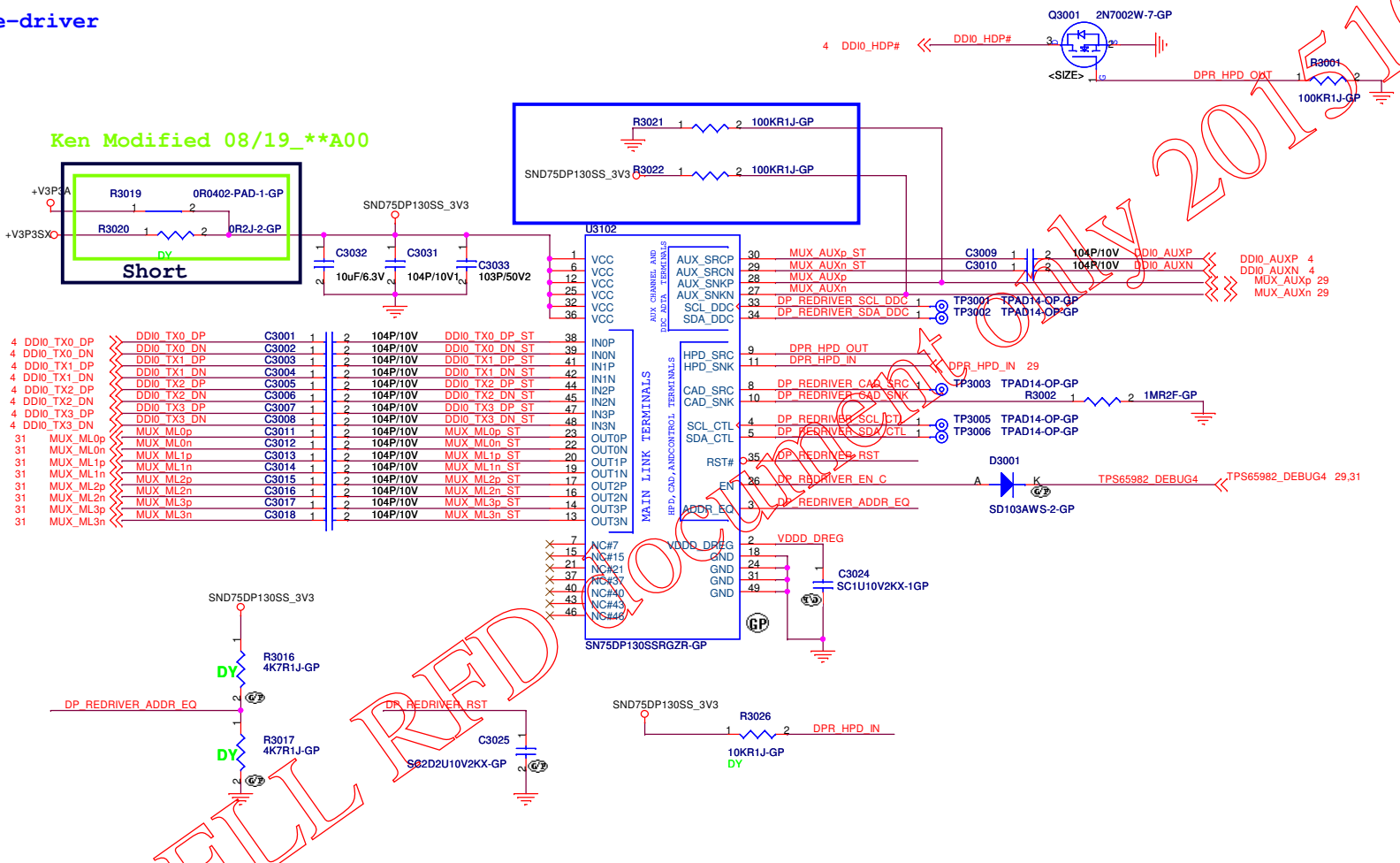
Rev
-1

73

SSID=VIDEO

Re-driver

Ken Modified 08/19_**A00



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Title **32_USB HUB(Reserved)**

Size	Document Number Blackwell T4	Rev -1
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Date: Thursday, October 01, 2015 Sheet 32 of 73

Vibrator

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Title

33_Vibrator(Reserved)

Size

Document Number

Blackwell T4

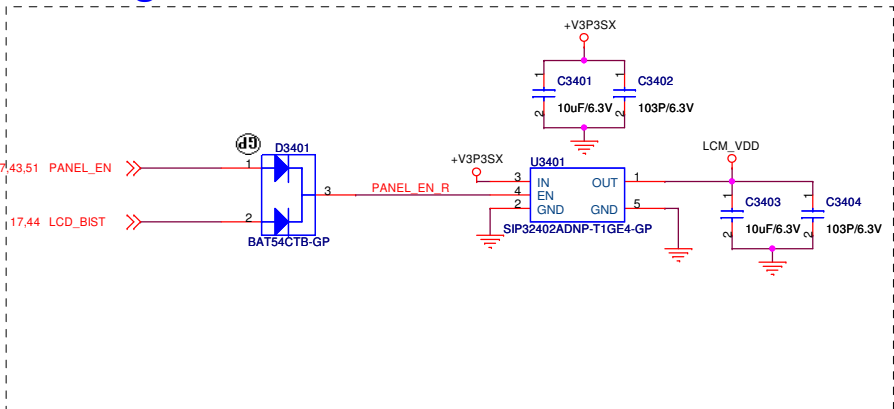
Rev

-1

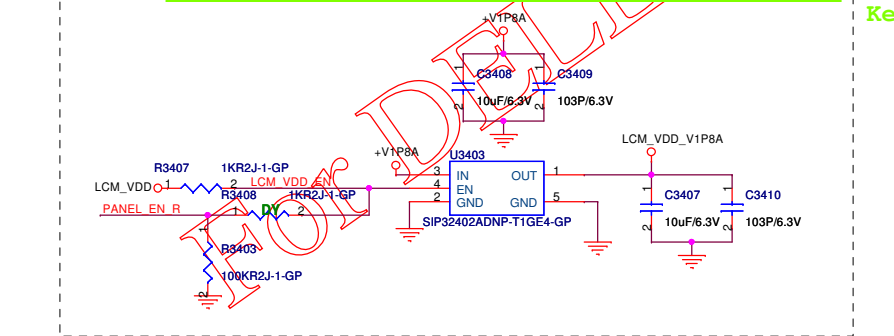
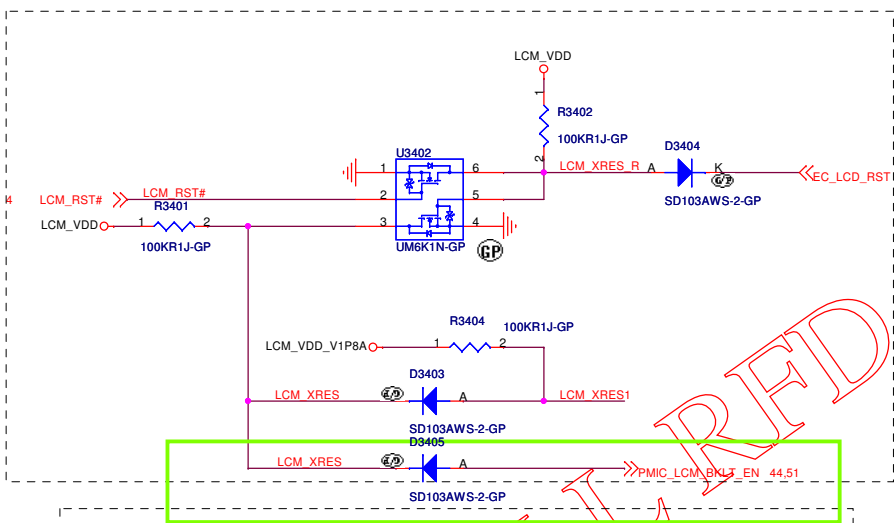
Date: Thursday, October 01, 2015

Sheet 33 of 73

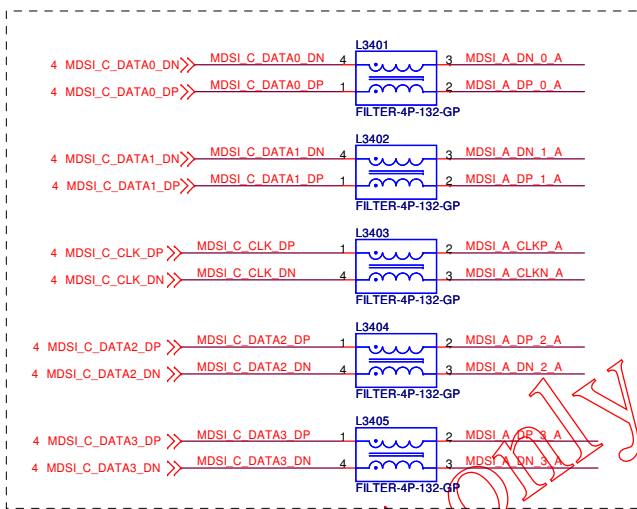
LCM Logic Power



Level Shift



For EMI

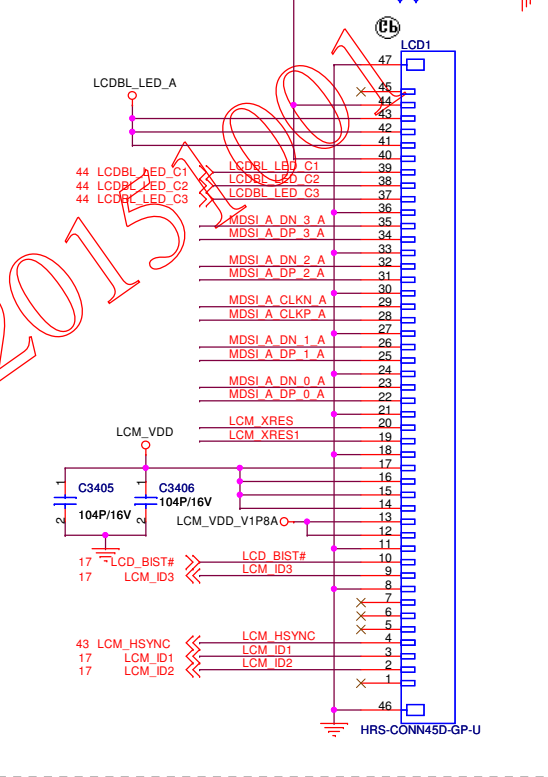


LCM ID 改的目的: 當EC 有電, 就可以偵測LCM是哪家

LCM_ID3	LCM_ID2	LCM_ID1	Vendor
0	0	0	
0	1	0	AUO-WUXGA
0	1	1	BOE-WUXGA
1	0	0	AUO-WUXGA
1	0	1	
1	1	0	BOE-WXGA
1	1	1	AUO-WXGA

Ken Modified 07/21_**A00

LCM Conector



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Title 34 MIPI LCM CONN

Size Document Number
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Date: Thursday, October 01, 2015

Sheet 34

of 73

Rev
-1

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Title		35_uHDMI CONN(Reserved)	
Size		Document Number	
Date: Thursday, October 01, 2015		Sheet 35 of 73	
Blackwell T4		Rev -1	

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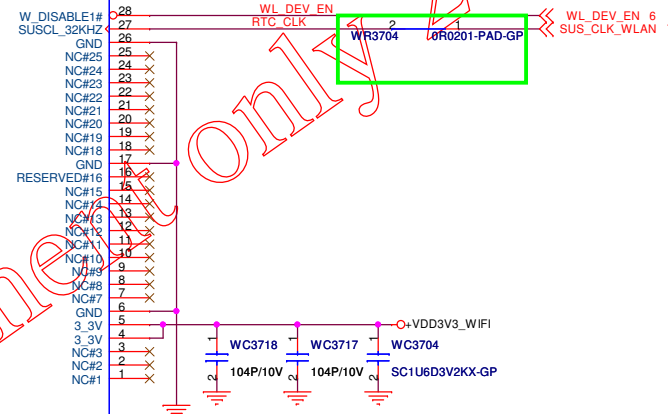
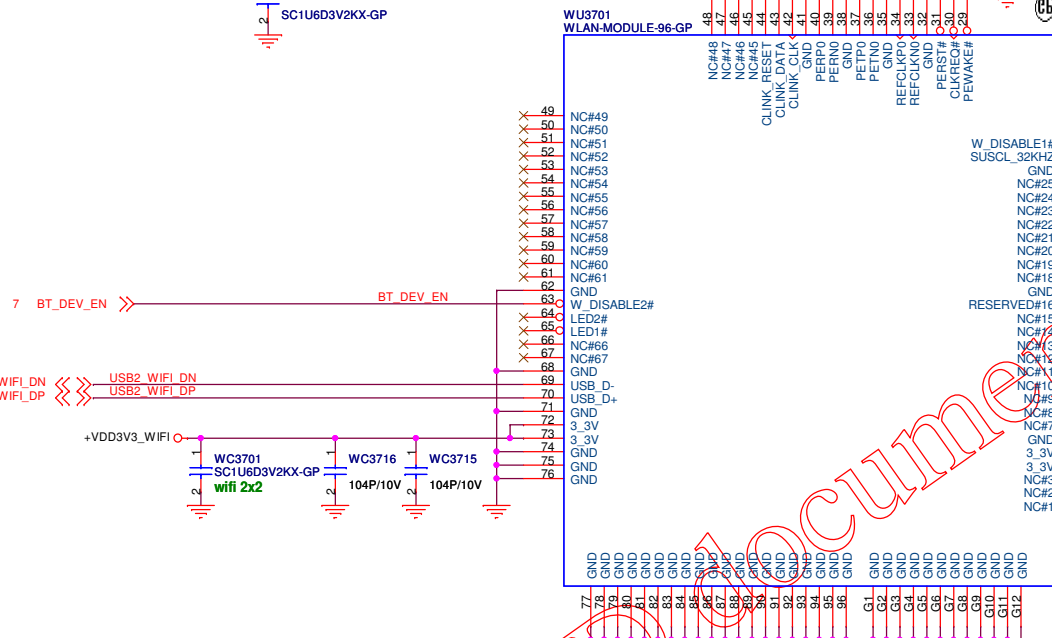
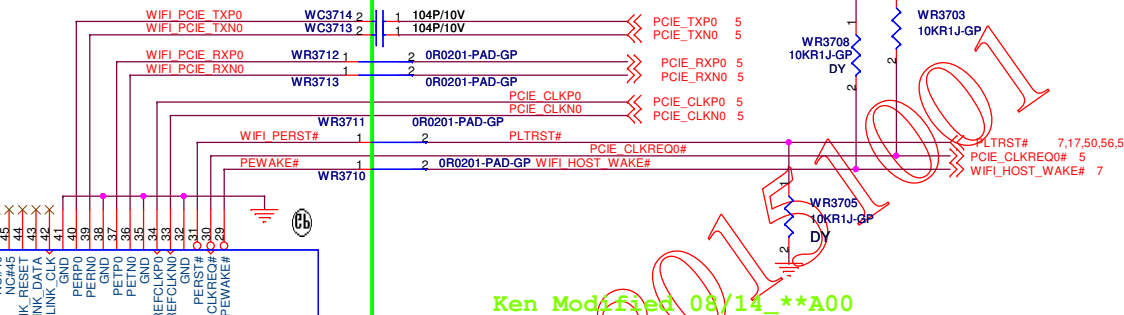
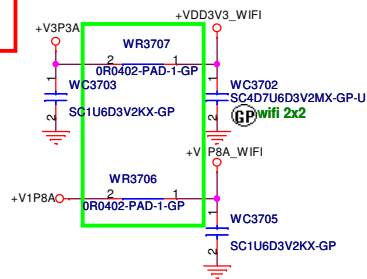
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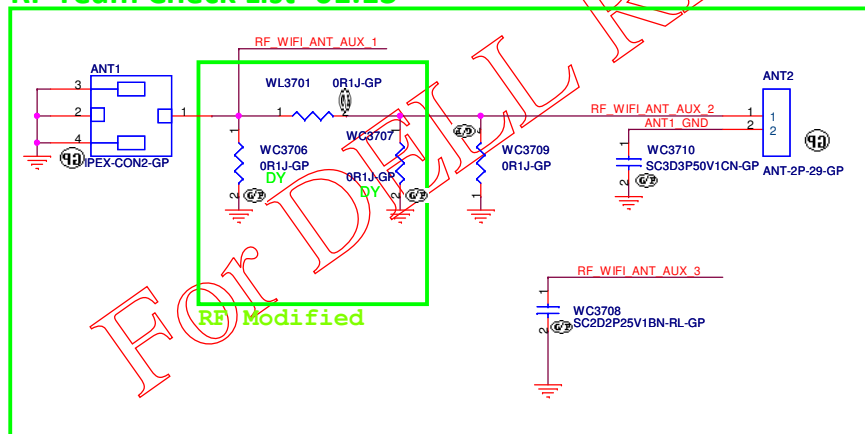
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Title 36_Display Port(Reserved)		
Size	Document Number	Rev
	Blackwell T4	-1
Date: Thursday, October 01, 2015		Sheet 36 of 73

WIFI/BT 2X2 US1

SSID=Wireless



RF Team Check List -01.13



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<Core Design>

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Title 37_WIFI/BT

Size Document Number
Blackwell T4

Date: Thursday, October 01, 2015

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Rev
-1

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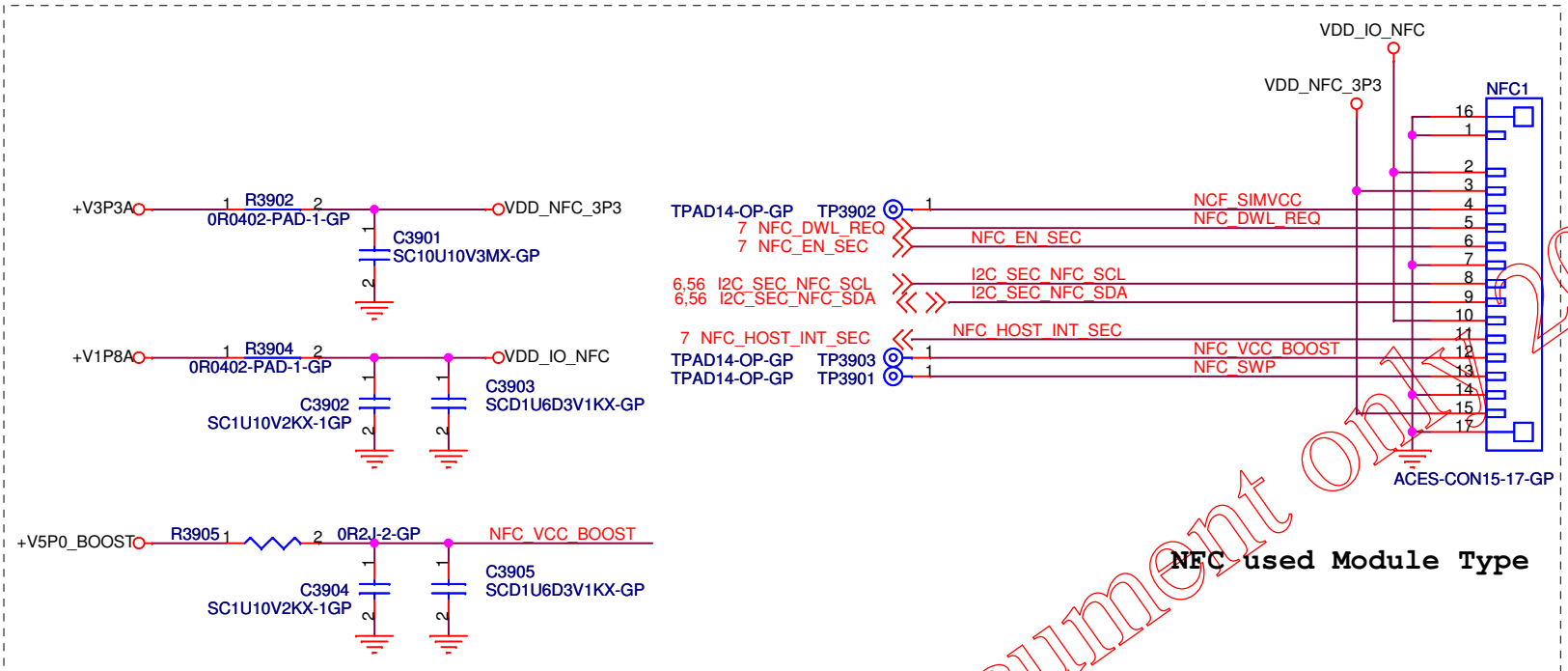
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Title 38_GPS(Reserved)		
Size	Document Number	Rev
	Blackwell T4	-1
Date: Thursday, October 01, 2015		Sheet 38 of 73

NFC

SSID=NFC



Pin number	Name
1	MOD_VDD
2	MOD_GND
3	SWP
4	VCC_BOOST
5	IRQ
6	PMUVCC
7	I ² C_SDA
8	I ² C_SCL
9	MOD_GND
10	Reset/Wakeup
11	DWL_REQ
12	SIMVCC
13	MOD_VDD
14	VDD_IO
15	MOD_GND

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Title
39_NFC

Size
Document Number
Blackwell T4

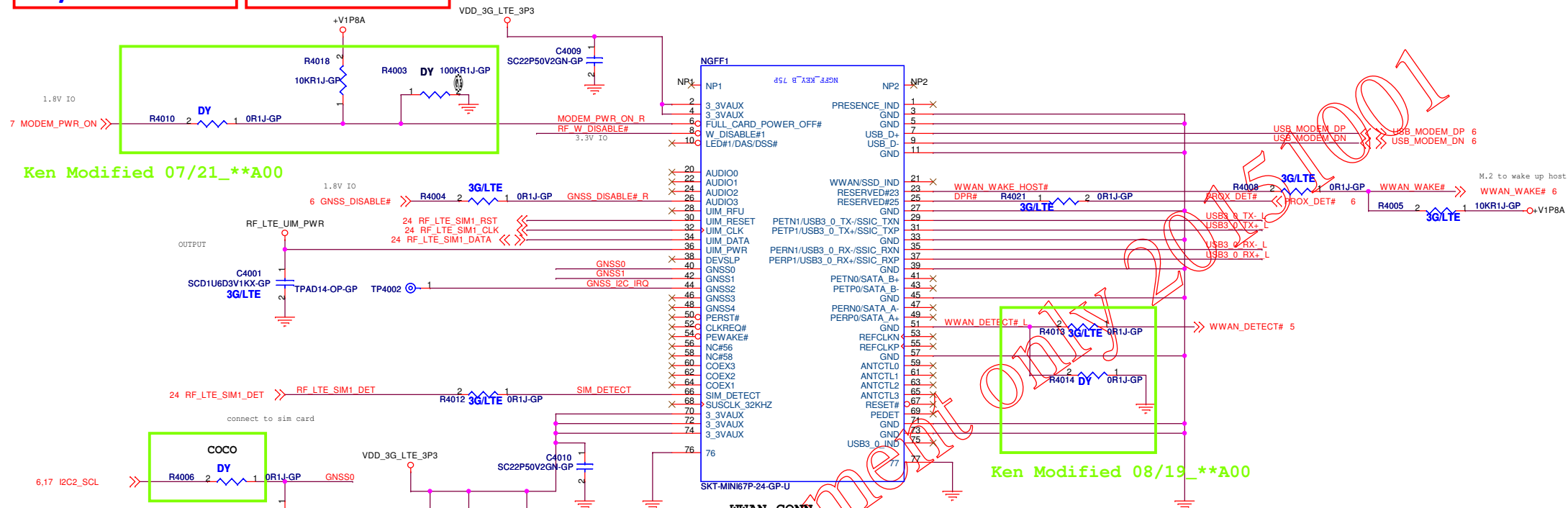
Rev
-1

Date: Thursday, October 01, 2015

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3G/LTE module

SSID=Wireless



6,17 I2C2_SCL >>> R4006 2 DY 1 0R1J-GP GNSS0

6,17 I2C2_SDA <<< R4007 2 DY 1 0R1J-GP GNSS1

COCO

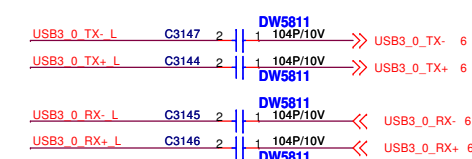
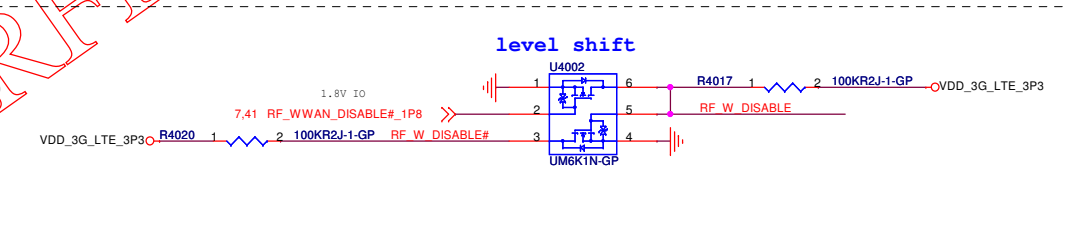
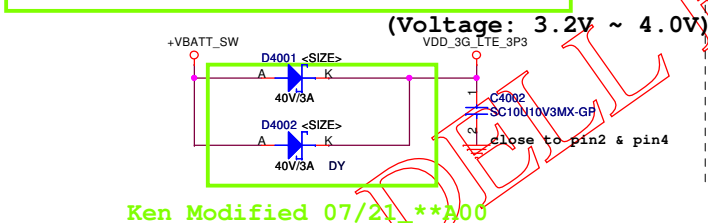
DW5811

Ken Modified 07/21_**A00

DW5811 EM7455 (Non COCO)

DW5808 EM7355 (COCO)

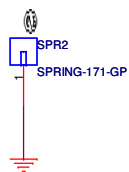
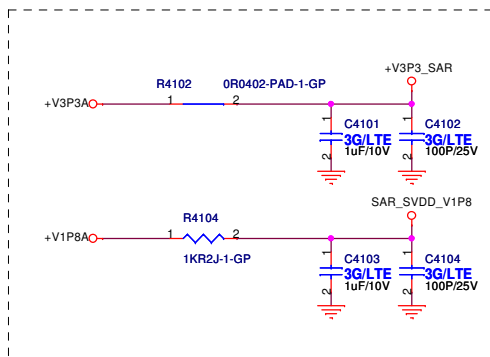
DW5809, DW5808: R4006, R4007, R4009: DY



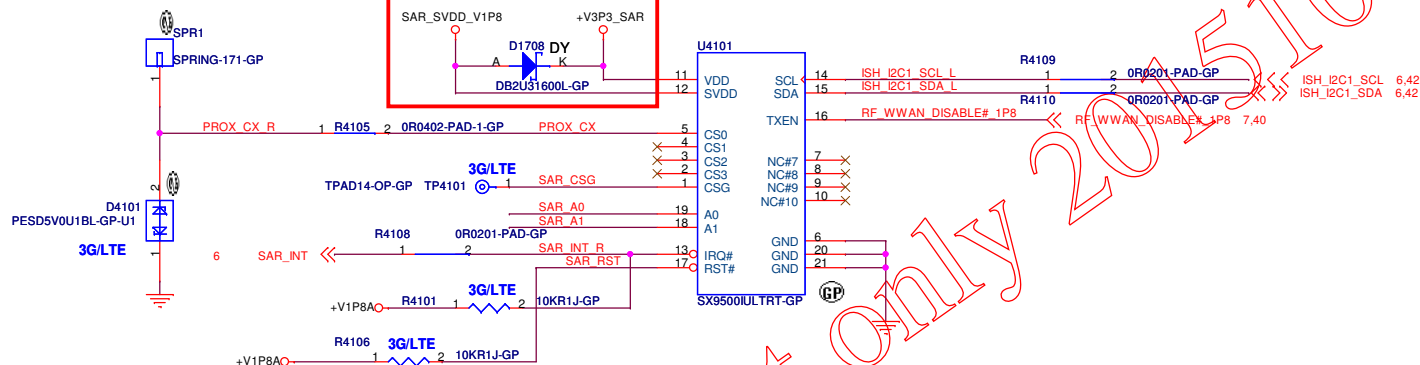
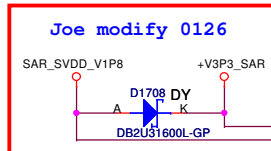
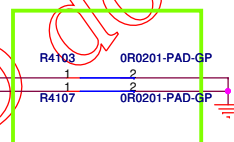
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SAR sensor for 3G/LTE

SSID=User.Interface



A1	A0	Address
0	0	0x28
0	1	0x29
1	0	0x2A
1	1	0x2B



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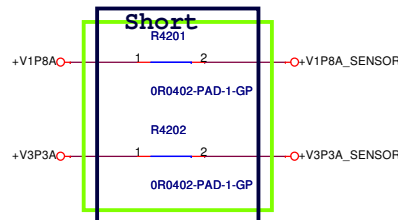
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Title	41_SAR Sensor		
Size	Document Number	Blackwell T4	Rev -1
Date	Thursday, October 01, 2015	Sheet 41 of 73	

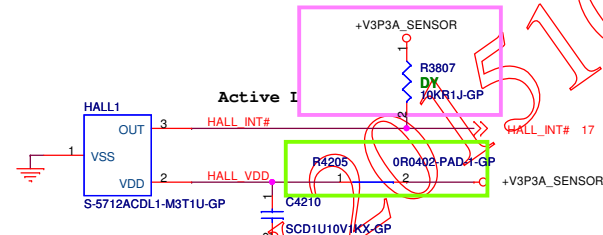
Sensor

SSID=User.Interface

Ken Modified 08/19_**A00

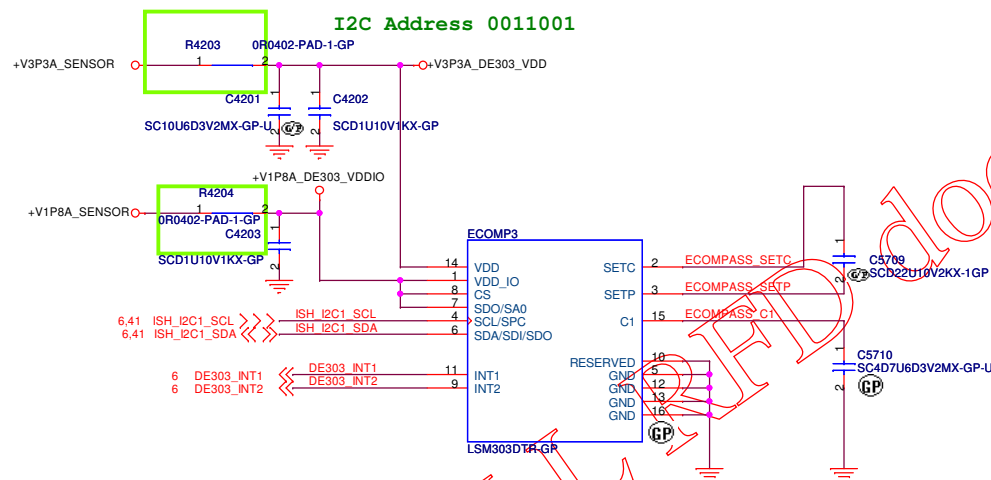


HALL Sensor

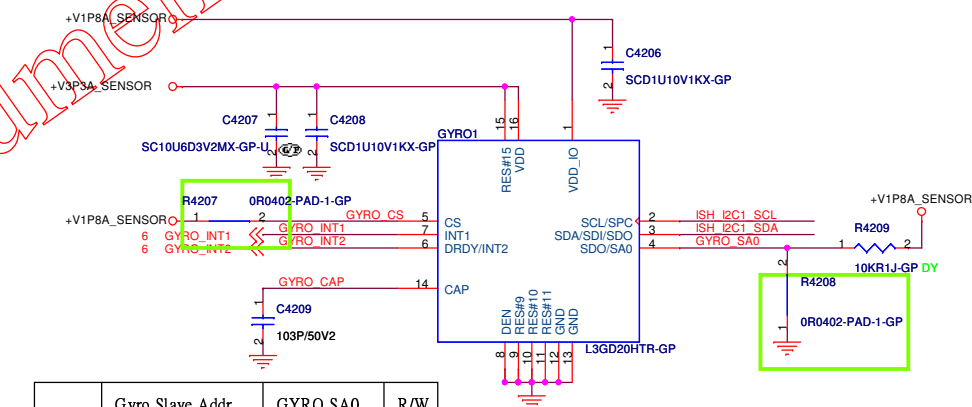


G Sensor + E-Compass

I2C Address 0011001



Gyro Sensor I2C Address 1101010



	Gyro Slave Addr	GYRO SA0	R/W
D4	Write	110101	0
D5	Read	110101	0

	G-Sensor Slave Addr	R/W
3A	Write	0011,101
3B	Read	0011,101

	c-Compass Slave Addr	R/W
3C	Write	0011,110
3D	Read	0011,110

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Title 42_Sensor

Size Document Number
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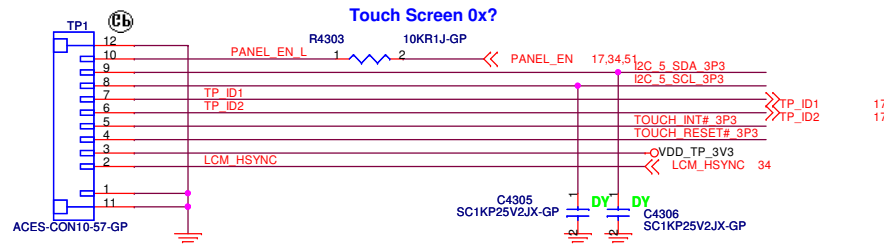
Date: Thursday, October 01, 2015

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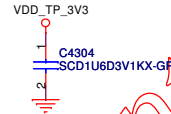
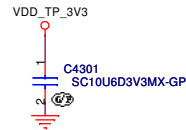
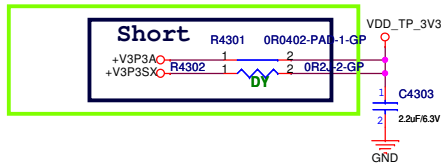
Rev
-1

Touch Panel

SSID=Touch.Panel

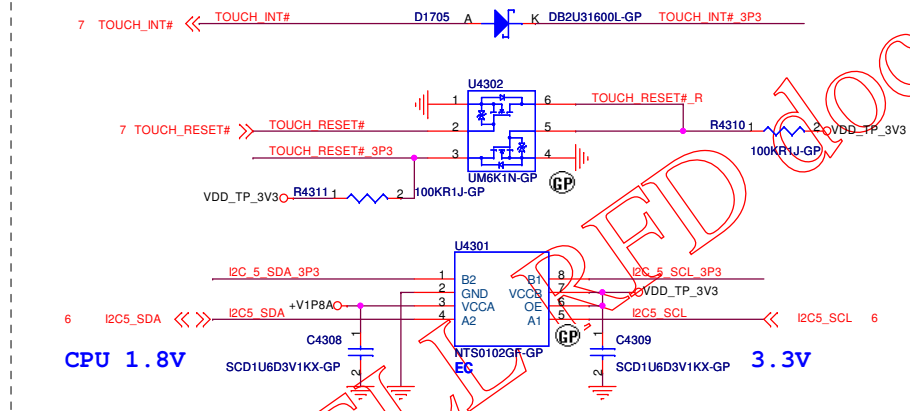


Ken Modified 08/19_**A00



CN1 PIN #	Host 接續時	Description
1	NC	Keep Open
2	SDA	IIC Data Open drain; pull-up resistor at Host is needed
3	SCL	IIC Clock Open drain; pull-up resistor at Host is needed
4	ID01	Touch Sensor Identification Pin 01
5	ID02	Touch Sensor Identification Pin 02
6	IRQ	IIC Data Ready Output "LOW" when data ready to send Open drain; pull-up resistor at Host is needed
7	RESET	RESET Stop operation when pull "LOW" Build-in pull-up resistor 100kohm
8	VDD +3.3V	3.3volt power input
9	HSYNC	LCD Hsync input
10	GND	Ground

Level shift



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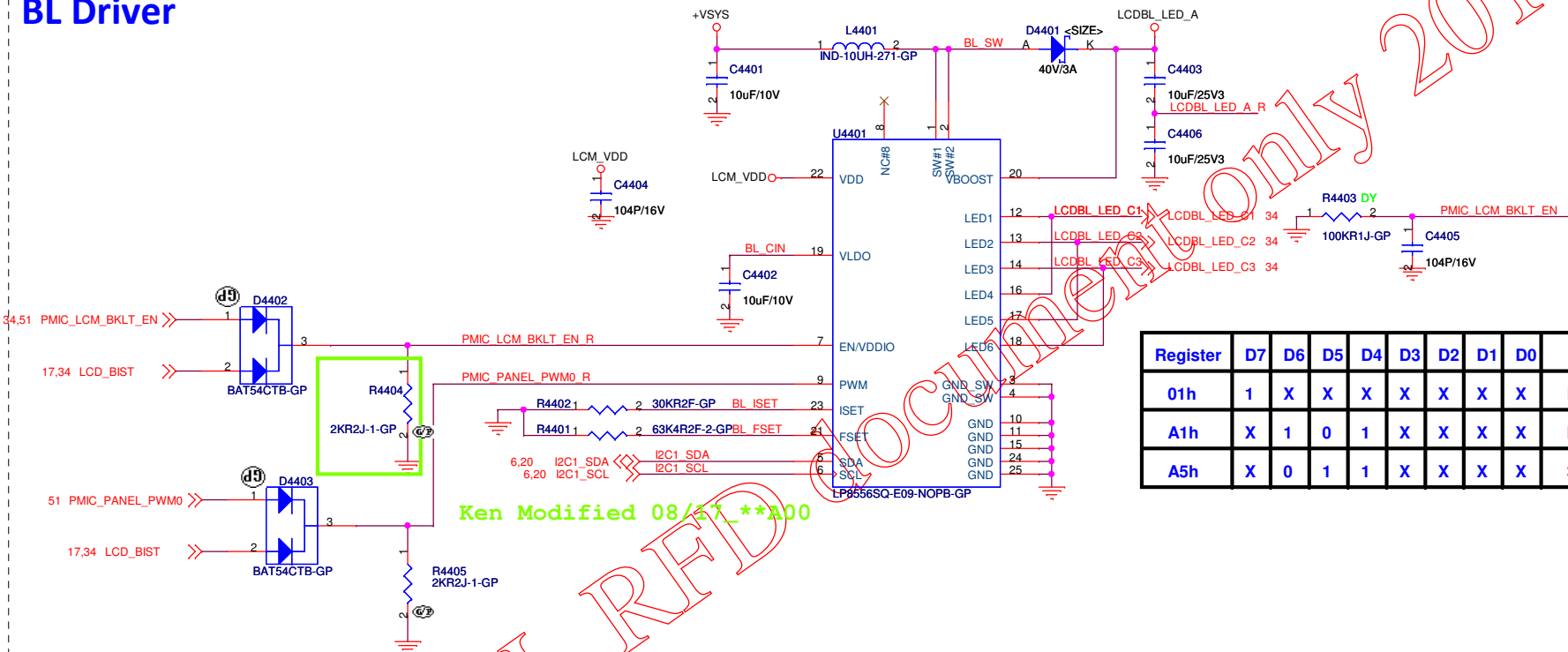
Blackwell T4

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Title	43_Touch Panel		
Size	Document Number	Rev	
	Blackwell T4	-1	
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SSID=VIDEO

BL Driver



Register	D7	D6	D5	D4	D3	D2	D1	D0	
01h	1	X	X	X	X	X	X	X	Don't update CFG from EEPROM
A1h	X	1	0	1	X	X	X	X	MAX current = 25mA
A5h	X	0	1	1	X	X	X	X	3-Phase,3 drivers

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Title 44_LED BOOST

Size B Document Number
Blackwell T4

Rev

-1

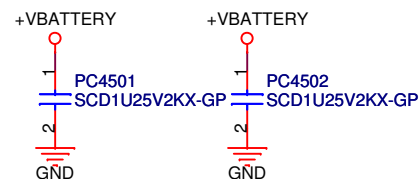
Date: Thursday, October 01, 2015

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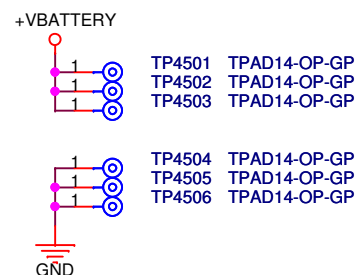
BATTERY CONN

SSID=PWR.Support

For EMI



For Test

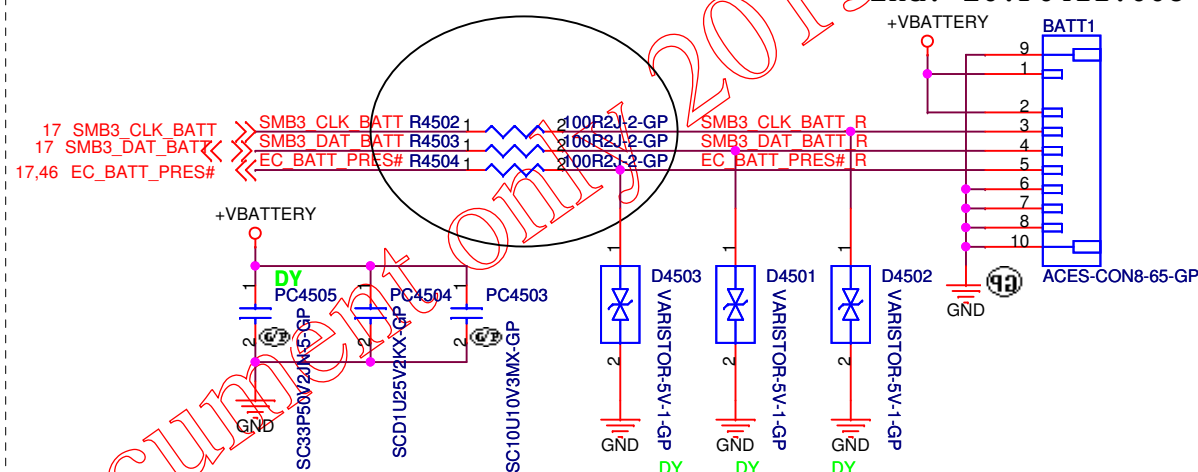


Battery Connector

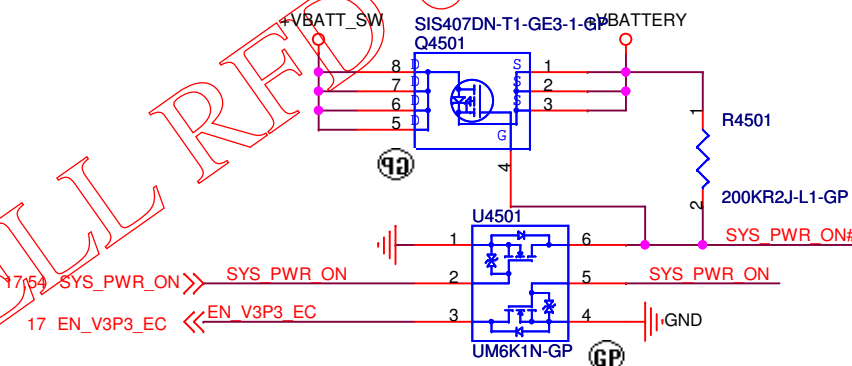
12.28 Ken Modified

Battery CONN

2nd: 20.F0411.008



S5/Shipping mode



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Title 45_BATT CONN

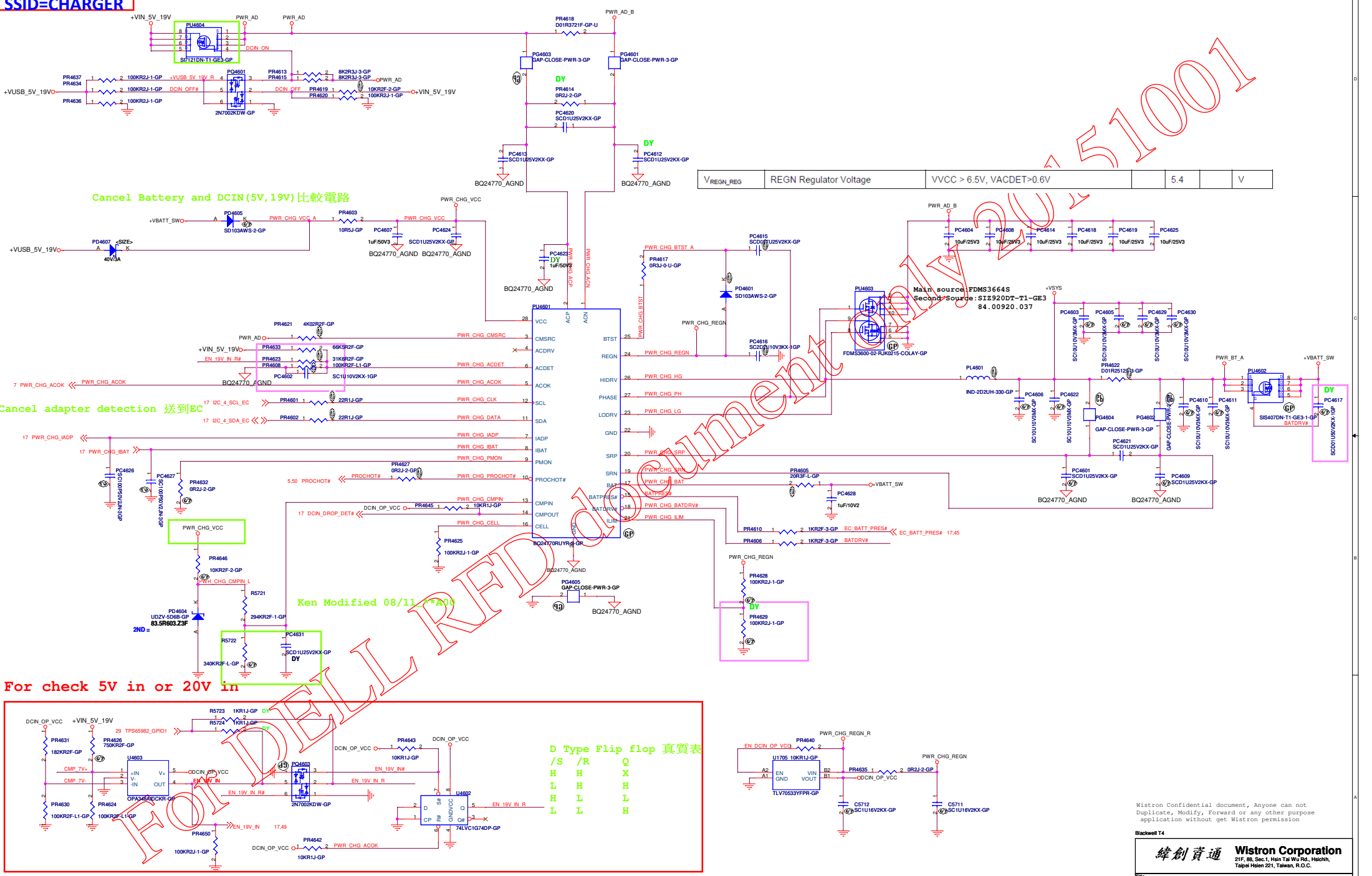
Size Document Number Blackwell T4

Date: Thursday, October 01, 2015

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Rev -1

Charger
SSID=CHARGER

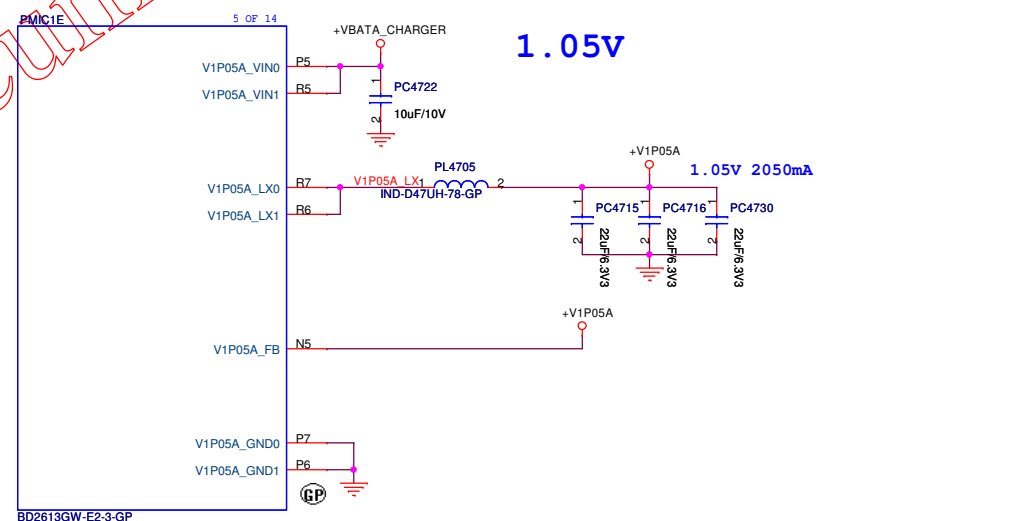
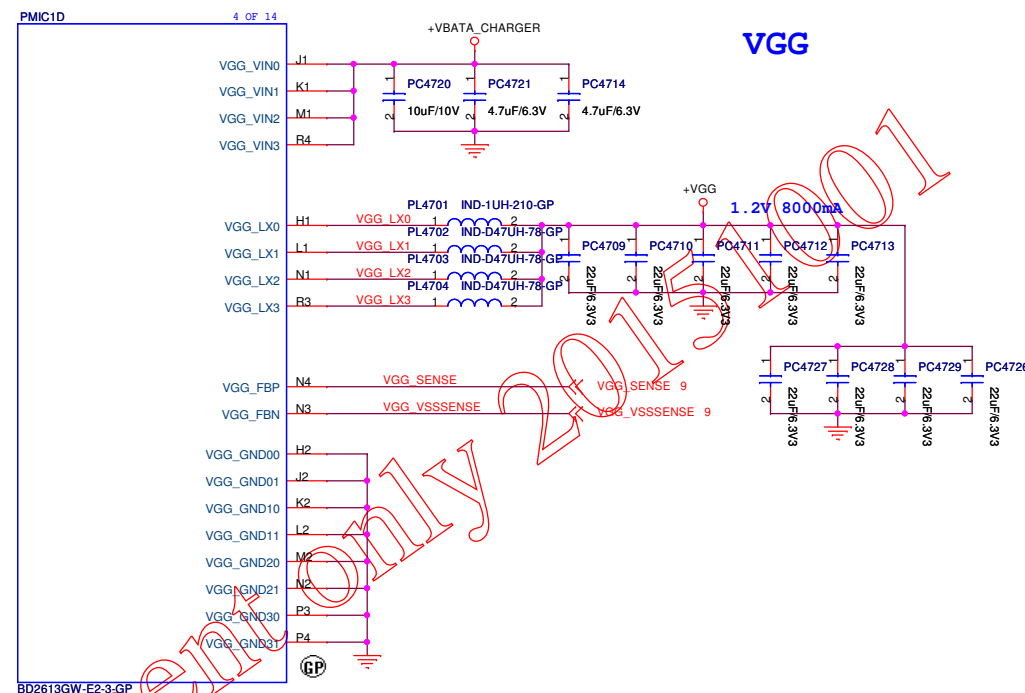
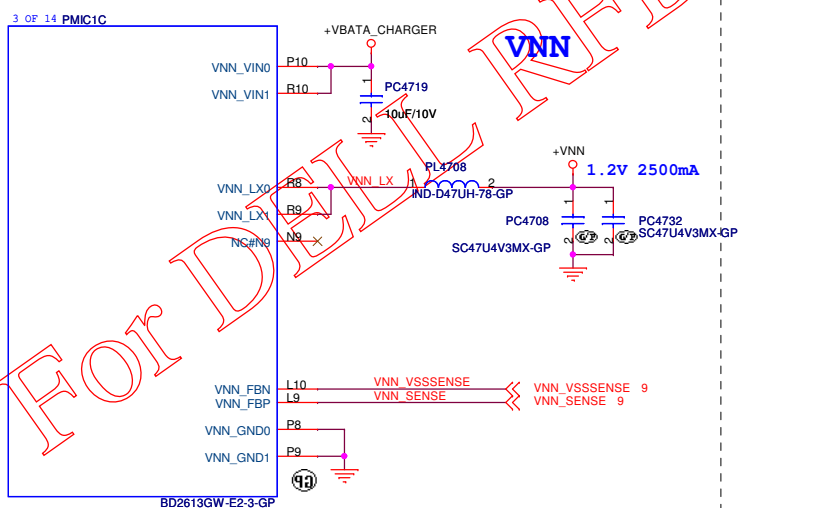
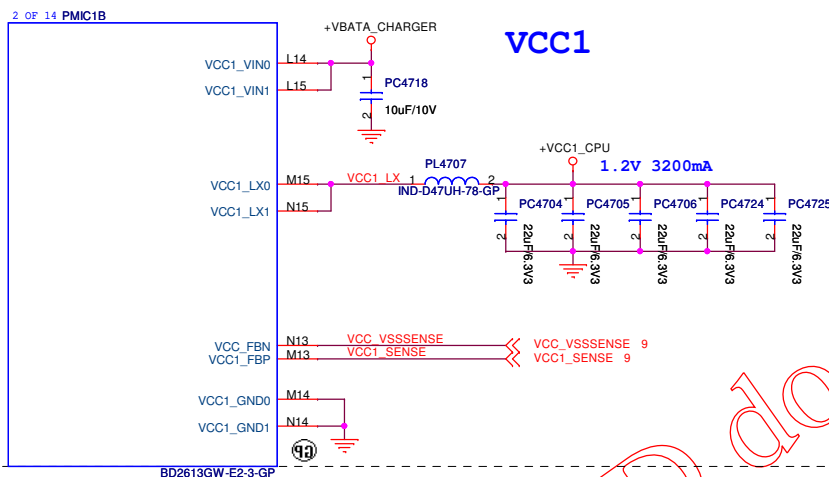
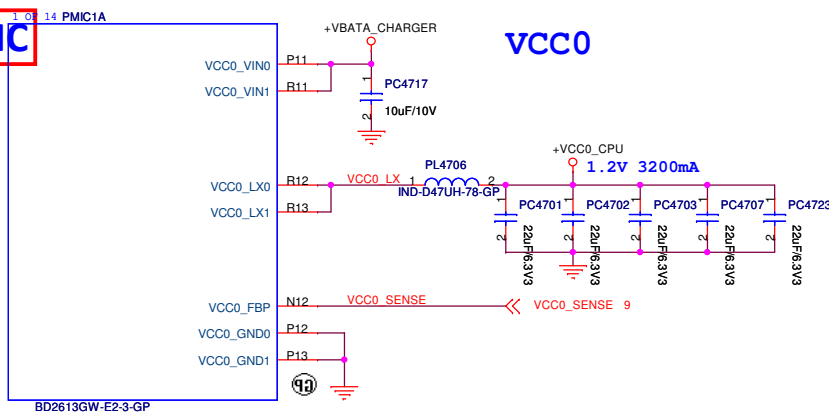


V _{REGN_REG}	REGN Regulator Voltage	V _{VCC} > 6.5V, V _{VACDET} > 0.6V	5.4	V
-----------------------	------------------------	---	-----	---

D Type Flip flop 真質表

/S	/R	Q
H	H	X
L	H	H
H	L	L
L	L	H

SSID=PMIC



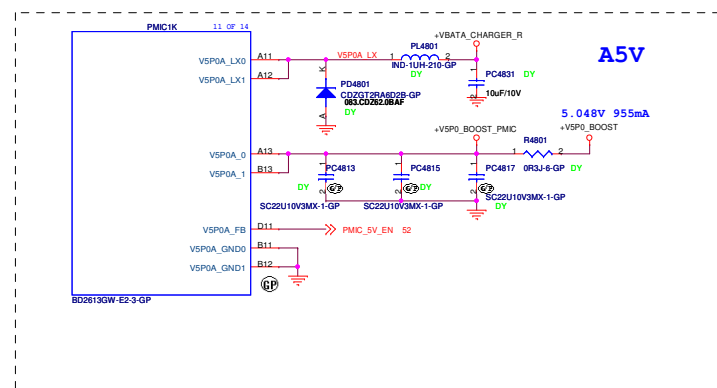
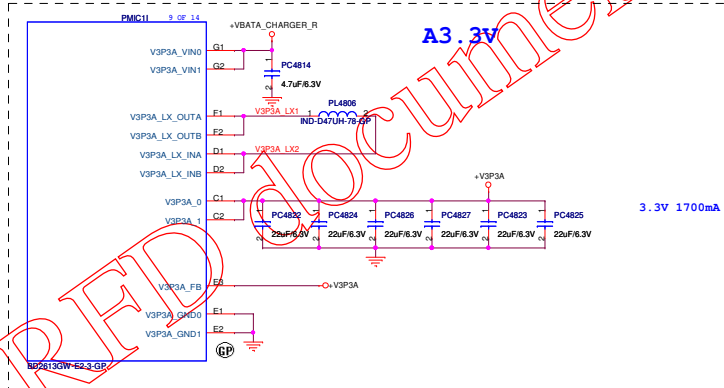
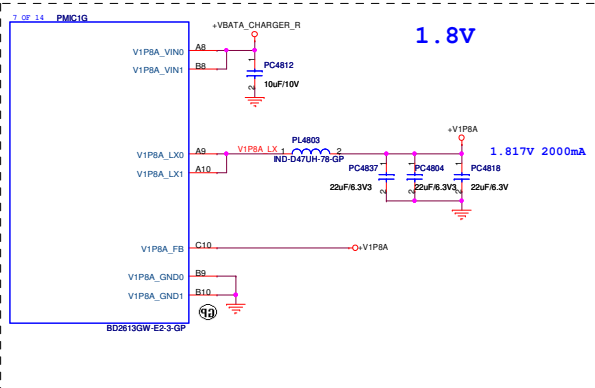
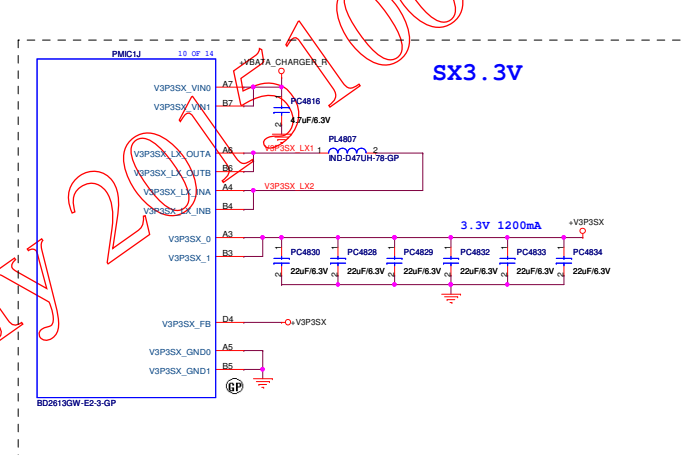
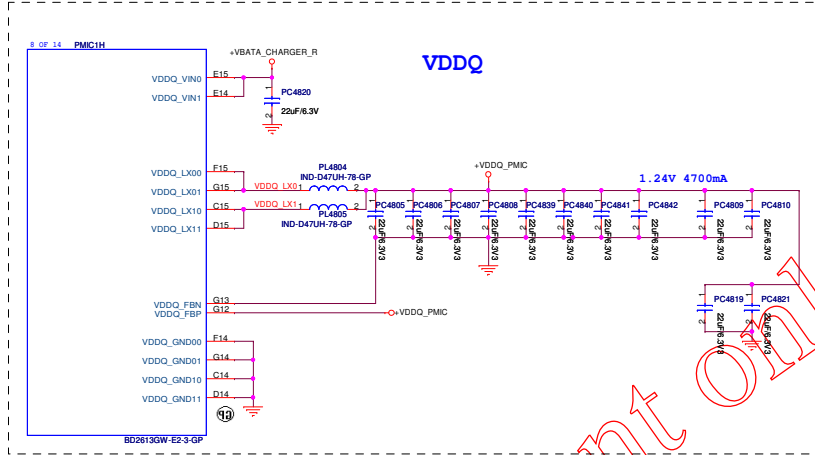
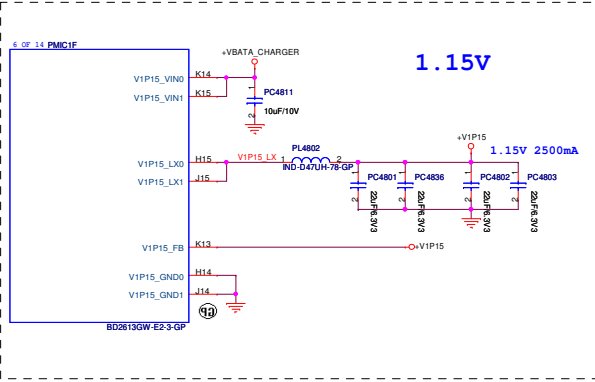
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Title		47 PMIC(1/5) (BD2613)	
Size	Document Number	Blackwell T4	
Date: Thursday, October 01, 2015	Sheet	47	of 73
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SSID=PMIC



Rohm PMIC decoupling amount target

	A1 Stepping	B0 Stepping
VCC0	5*47uF	3*47uF
VCC1	5*47uF	3*47uF
VNN	4*47uF	2*47uF
VGG	4*47uF	4*47uF
VGG	6*22uF	4*22uF
V1P05A	4*47uF	1*47uF
VIP15	4*47uF	2*47uF
V1P8A	5*22uF	3*22uF
VDDQ	8*47uF	6*47uF
V3P3A	10*47uF	4*47uF
V3P3SX	8*47uF	4*47uF
V5P0A	6*10uF	6*10uF

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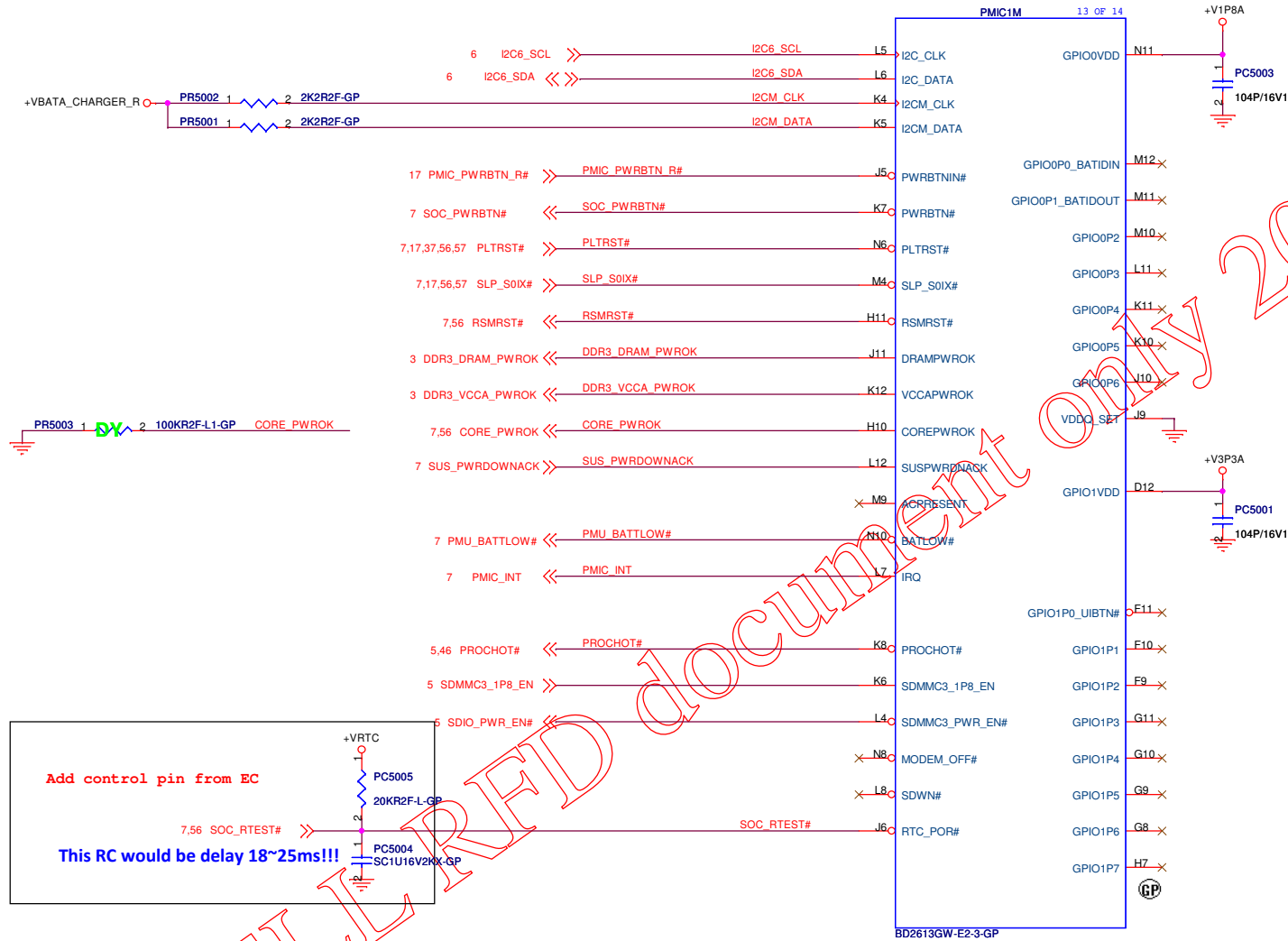
緯創資通 Wistron Corporation
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File: **48 PMIC(2/5) (BD2613)**
Size: **Blackwell T4**
Date: Thursday, October 01, 2015 Sheet: 48 of 73 Rev: -1

[illegible]

Title			
49 PMIC(3/5) (BD2613)			
Size	Document Number		Rev
	Blackwell T4		-1
Date:	Thursday, October 01, 2015	Sheet 49 of	73

SSID=PMIC



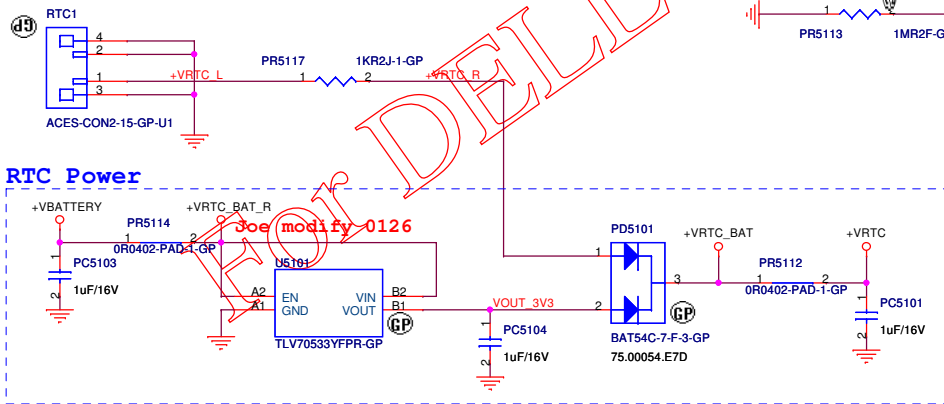
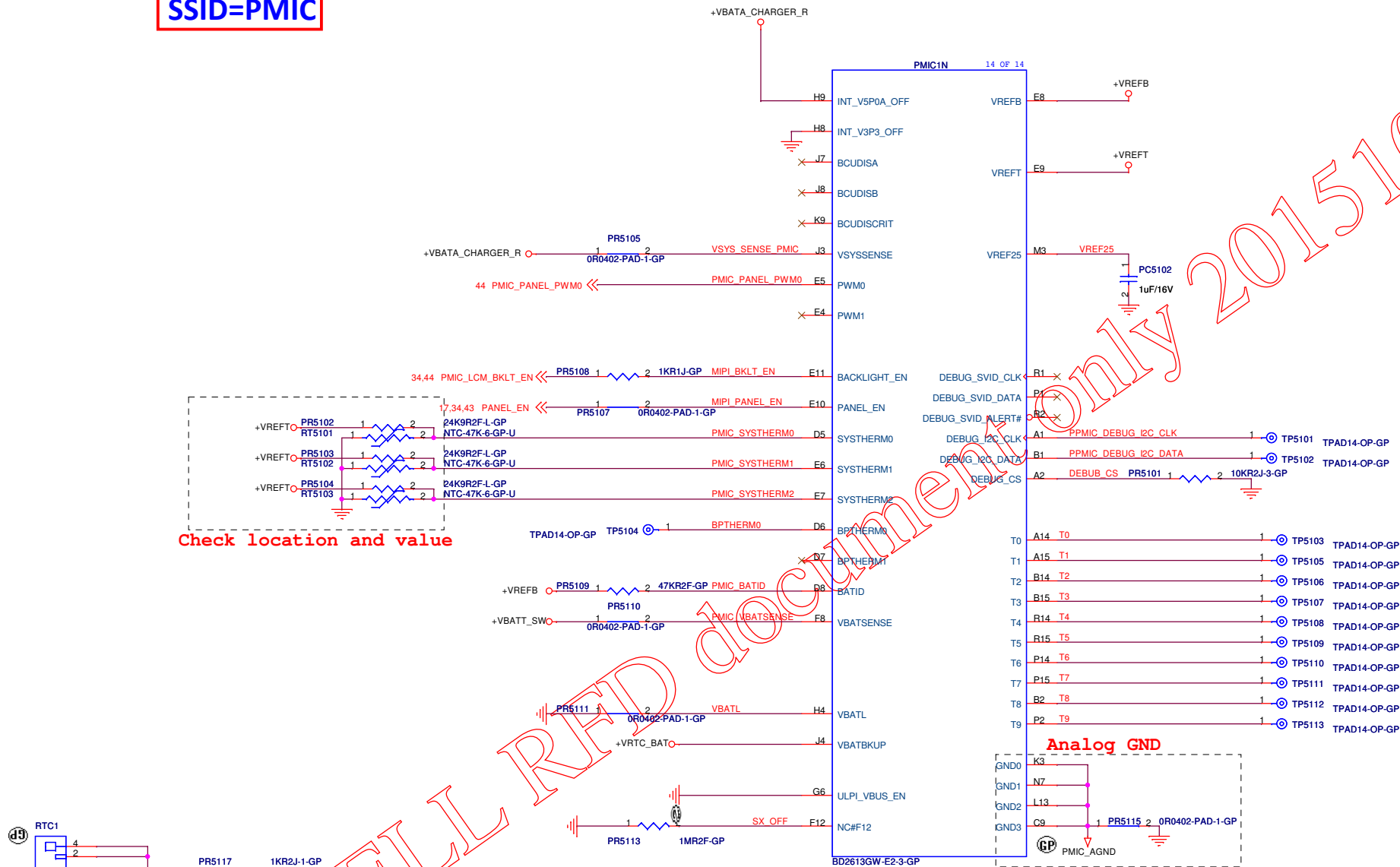
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Title			50 PMIC(4/5) (BD2613)
Size	Document Number	Rev	
	Blackwell T4	-1	
Date:	Thursday, October 01, 2015	Sheet	50 of 73

SSID=PMIC



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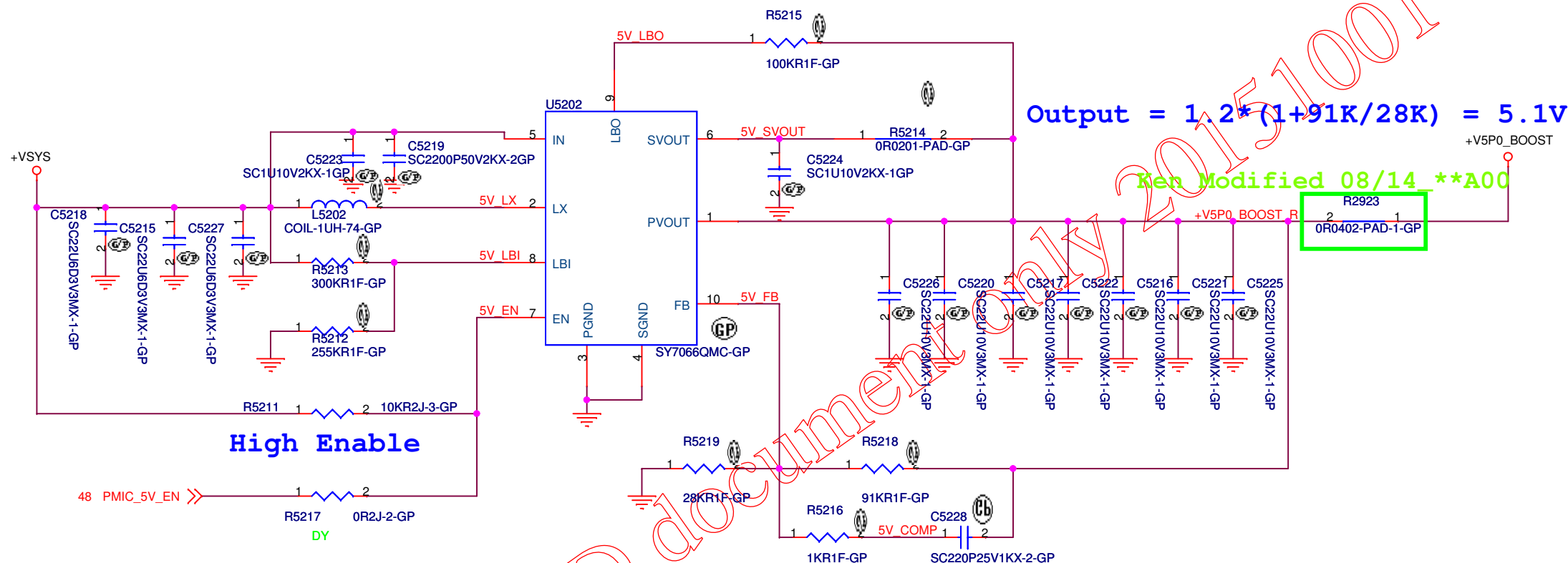
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Title	51_PMIC(5/5)_(BD2613)
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Size	Document Number Blackwell T4	Rev -1
Date:	Thursday, October 01, 2015	Sheet 51 of 73

SSID=PWR.Plane.Regulator_5v



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Title	52 5V BOOST & 3.3V(Reserved)
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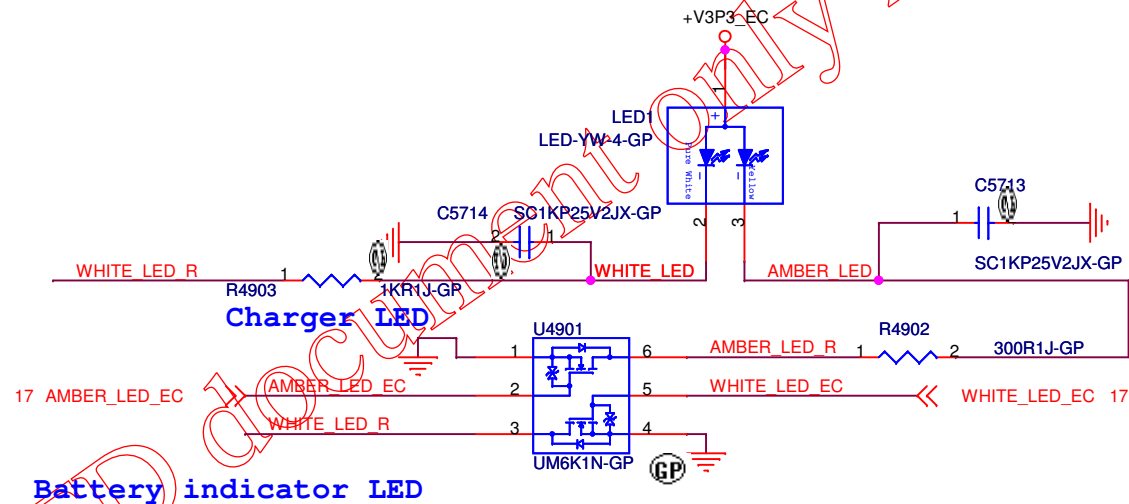
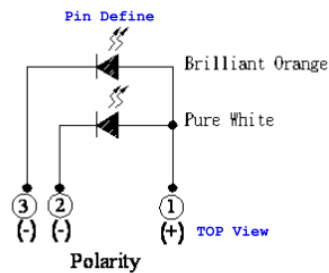
Size	Document Number Blackwell T4
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Rev	-1
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Date: Thursday, October 01, 2015 Sheet 52 of 73

POWER/Charger LED

SSID=User.Interface



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Title **53_POWER LED/DOCK CONN**

Size Document Number
Blackwell T4

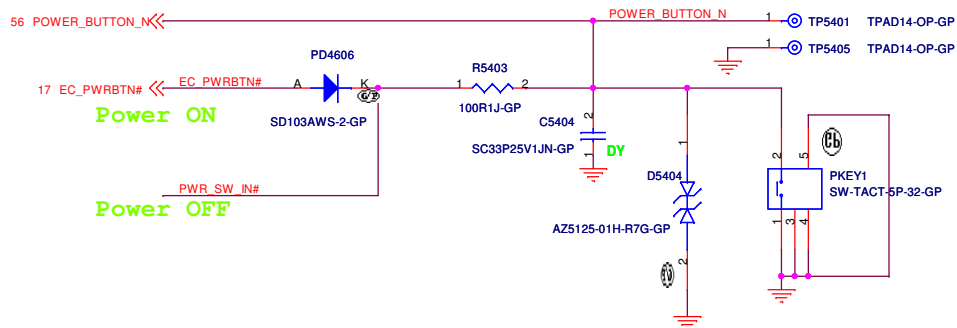
Rev
-1

Date: Thursday, October 01, 2015 Sheet 53 of 73

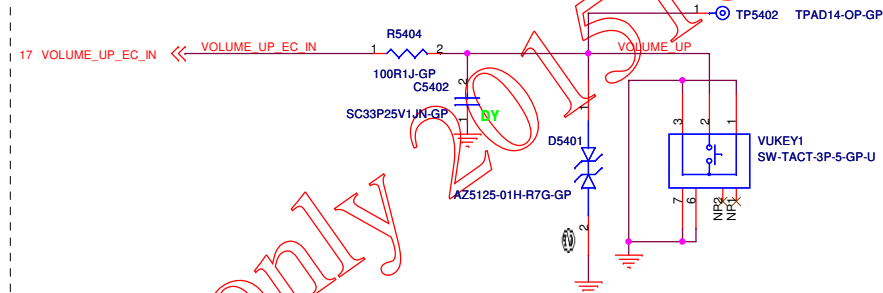
PWR Button / Volum Key / Home key

SSID=User.Interface

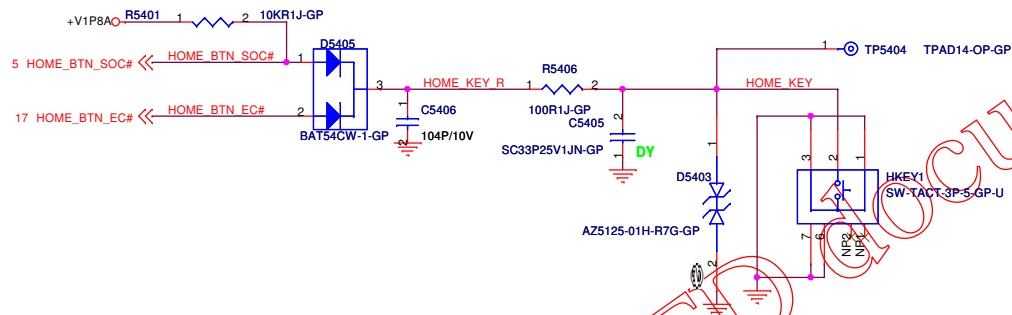
POWER KEY



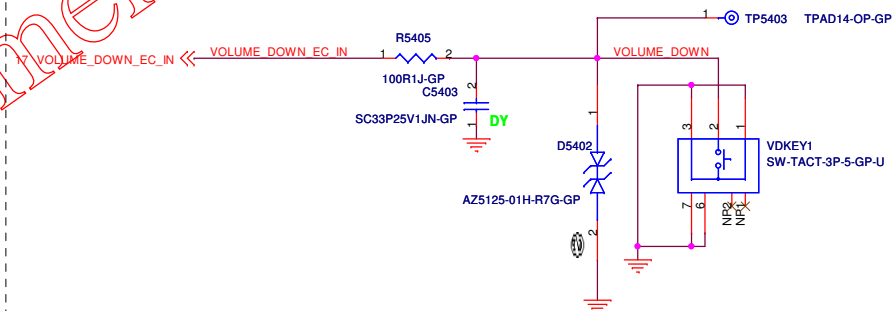
VOLUME UP KEY



HOME KEY

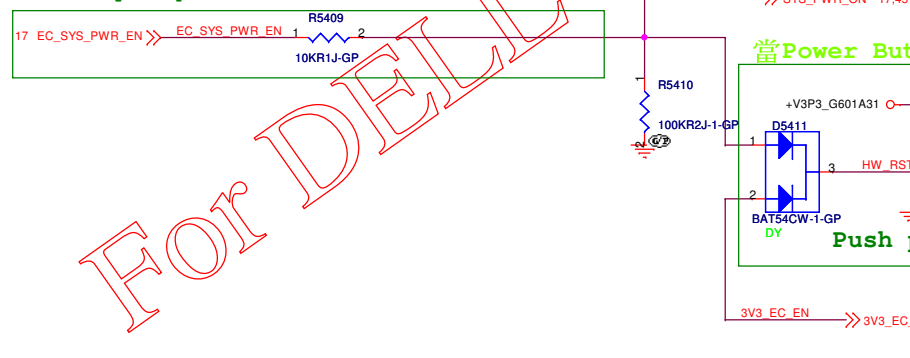


VOLUME DOWN KEY



SYSTEM POWER ON

EC latch System power on



當Power Butoton 按下時,Reset#為LOW,Power Button 放開時,Reset#為Hgh.

Push power button 15s, system power off

當長按16S, System Power off

$T = 76000 \times 0.22\mu F$
 $= 16.72ms$

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Title 54_PWR/Volume/Home Button		
Size	Document Number Blackwell T4	Rev -1
Date: Thursday, October 01, 2015	Sheet 54	of 73

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Title

55_IO Board Connector(Reserved)

Size

Document Number

Rev

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-1

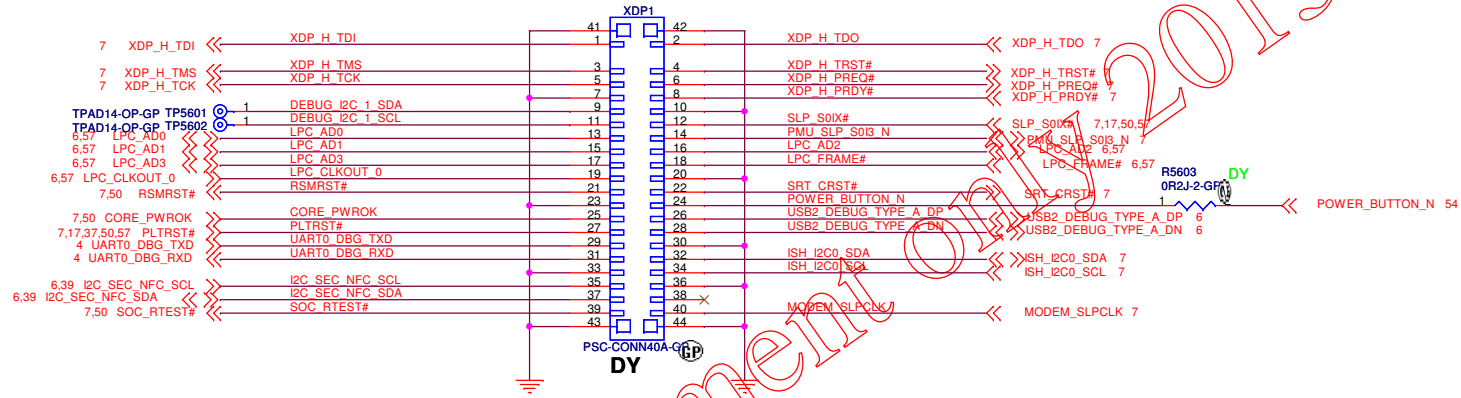
Date: Thursday, October 01, 2015

Sheet 55 of 73

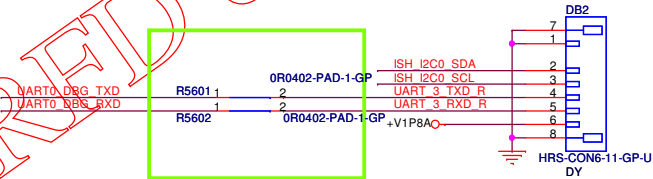
XDP Debug Connector

SSID=XDP

Debug Connector with XDP



SW Debug Connector



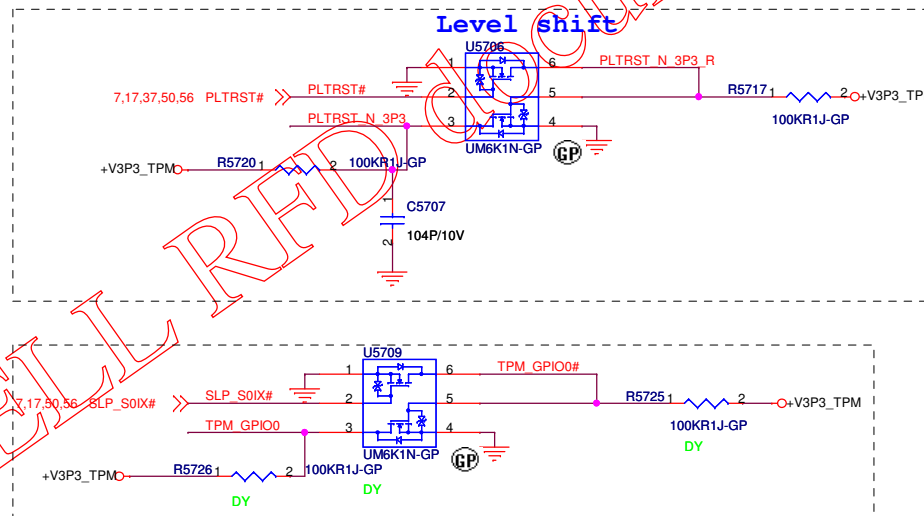
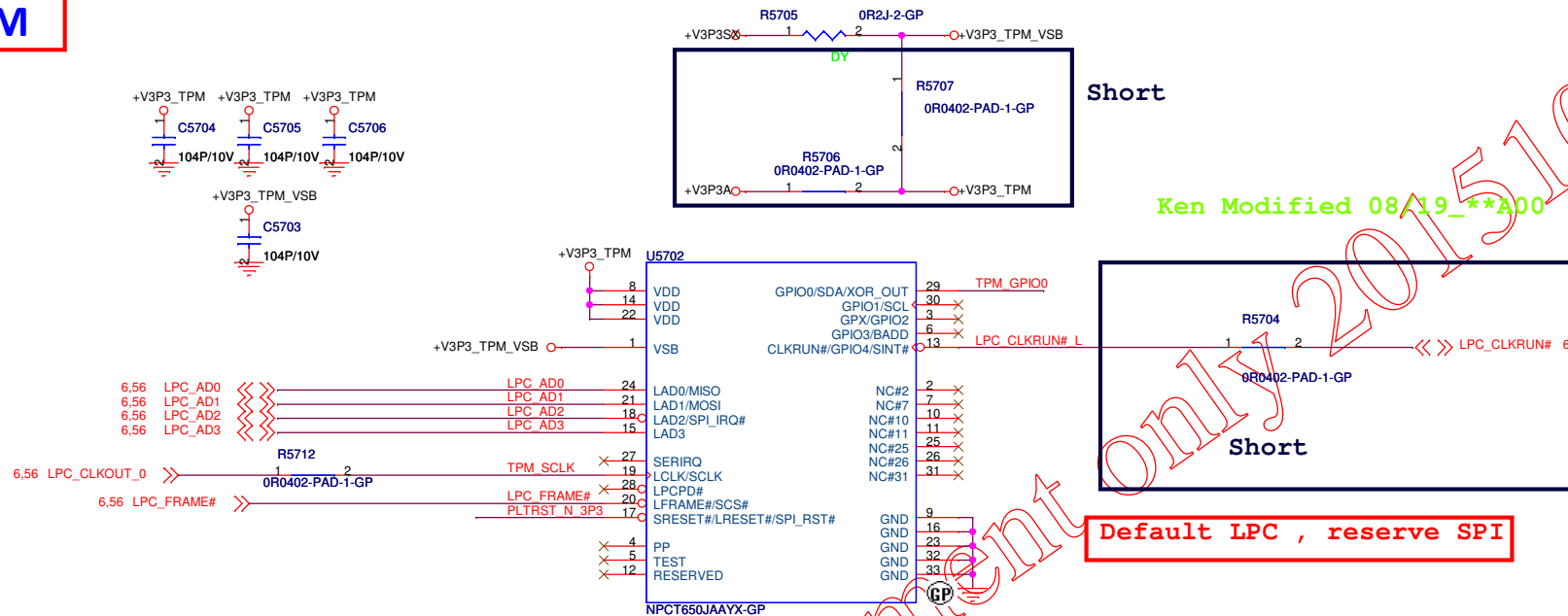
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Title		56_XDP Connector
Size	Document Number	Blackwell T4
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SSID=TPM



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Title	57 TPM		
Size	Document Number	Rev	
	Blackwell T4	-1	
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Title

58_Docking Connector(Reserved)

Size

Document Number

Blackwell T4

Rev

-1

Date: Thursday, October 01, 2015

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Title

59_CPU_XDP(Reserved)

Size

Document Number

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Rev

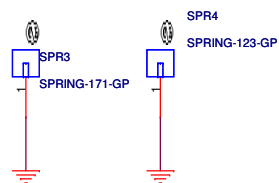
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Date: Thursday, October 01, 2015

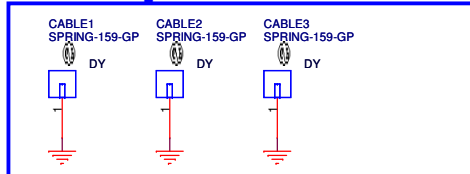
Sheet 59 of 73

Shielding Can

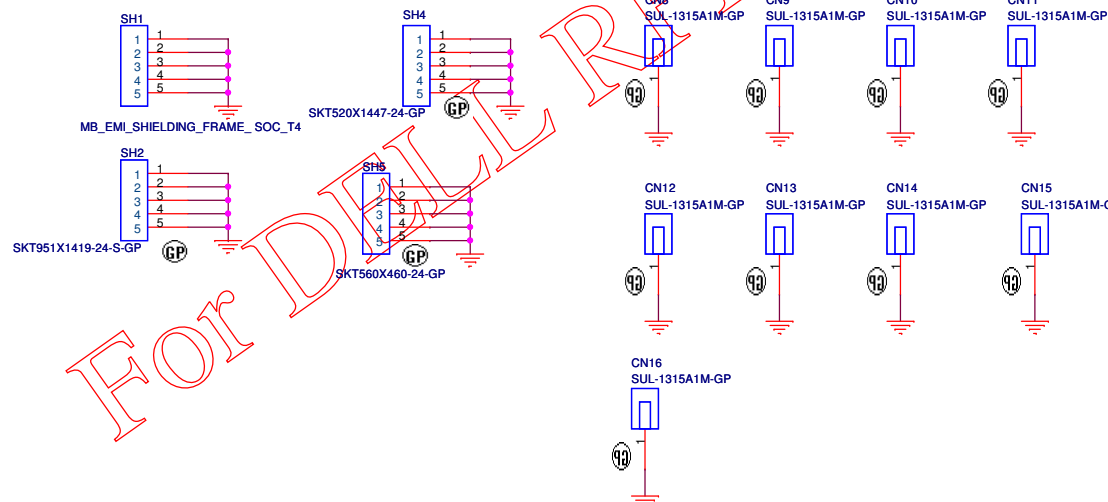
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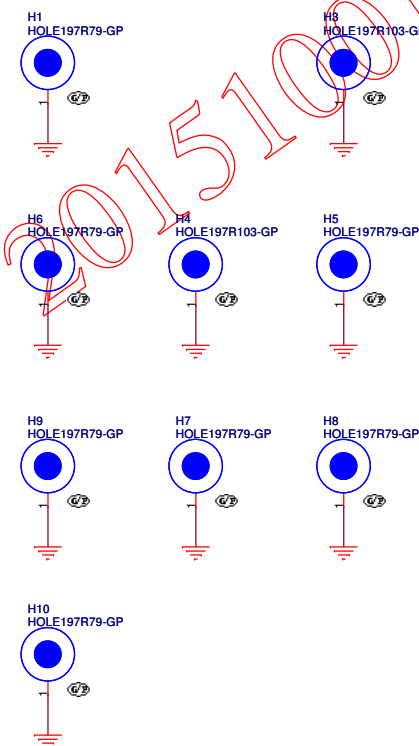
Joe modify 0114



Joe modify 0114



Screw Hole



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Title	60_ME/EMI		
Size	Document Number	Rev	
	Blackwell T4	-1	
Date: Thursday, October 01, 2015	Sheet 60	of	73

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Title

61_RF(Reserved)

Size

Document Number

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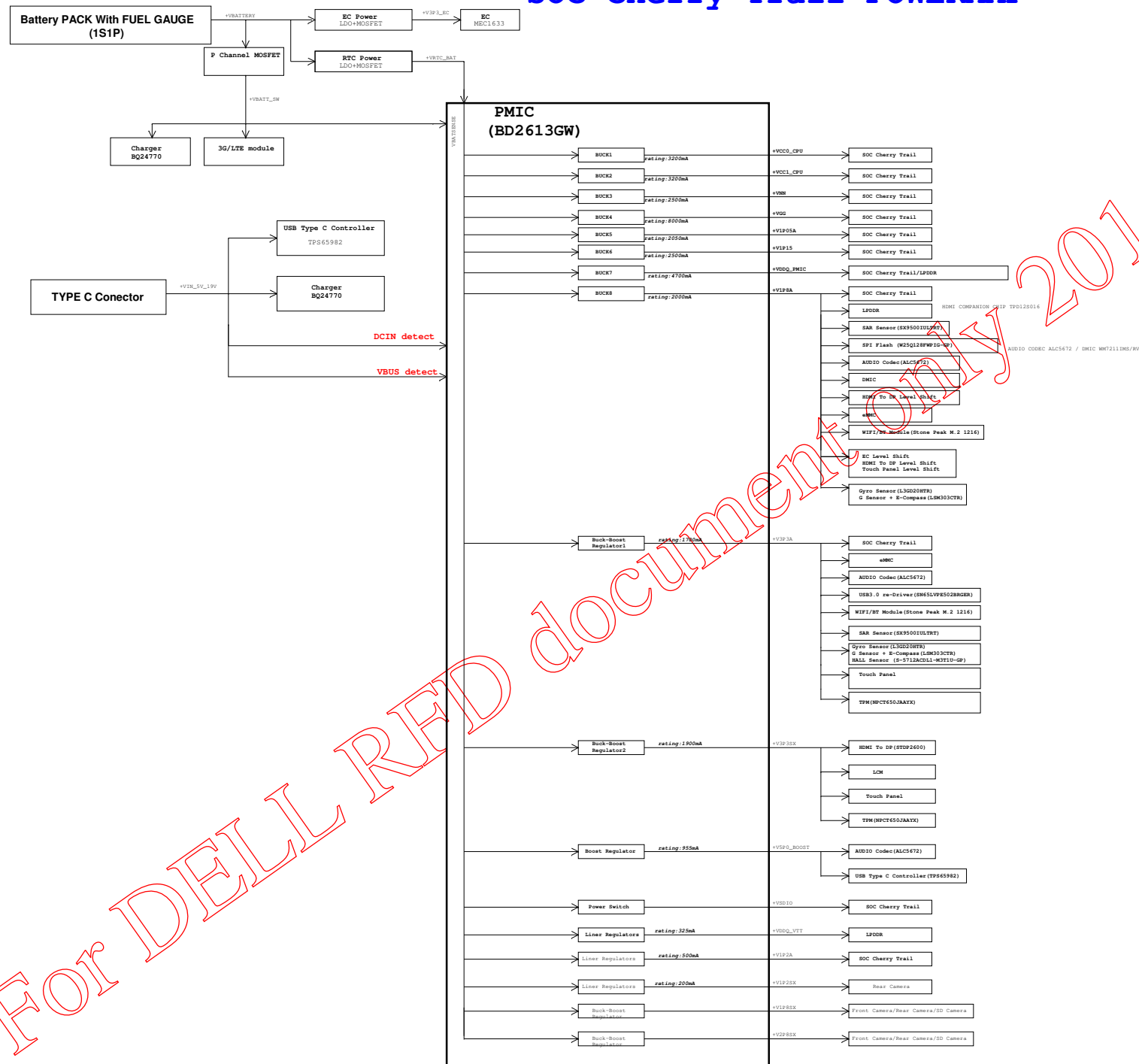
Rev

-1

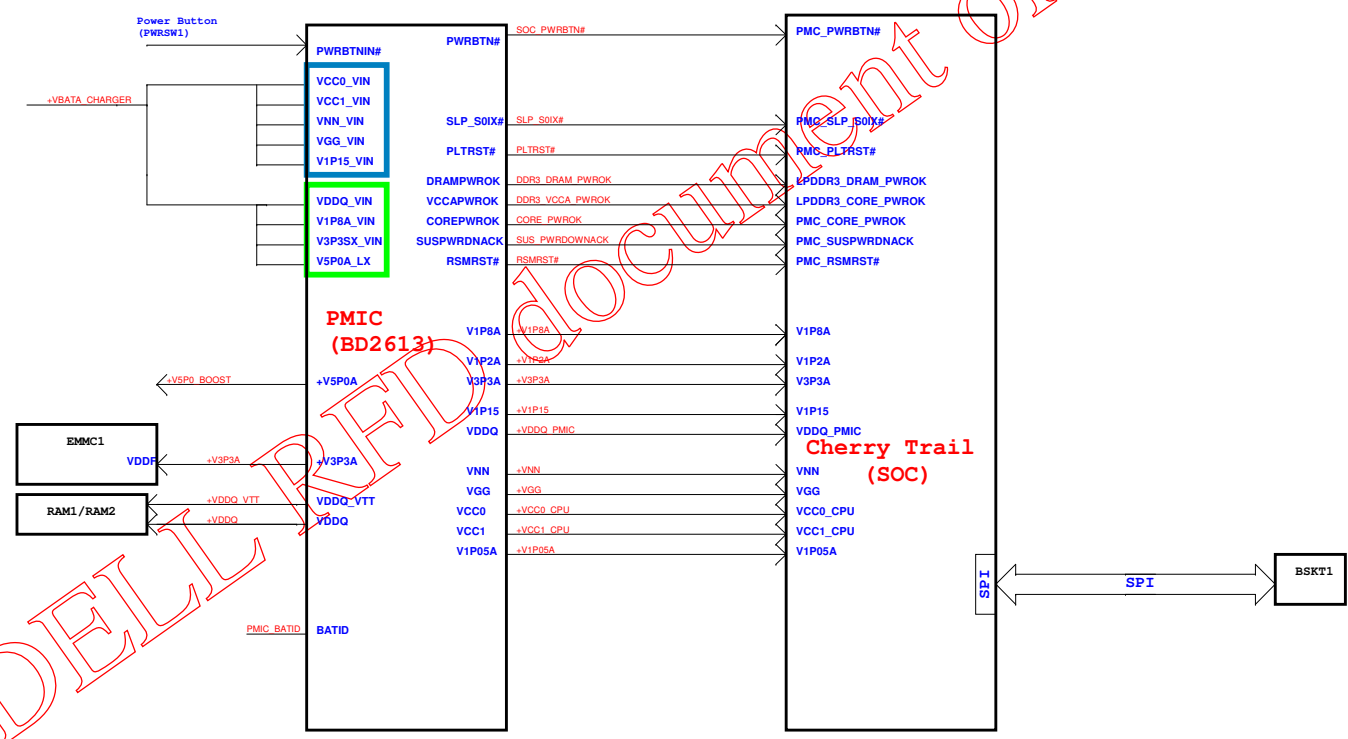
Date: Thursday, October 01, 2015

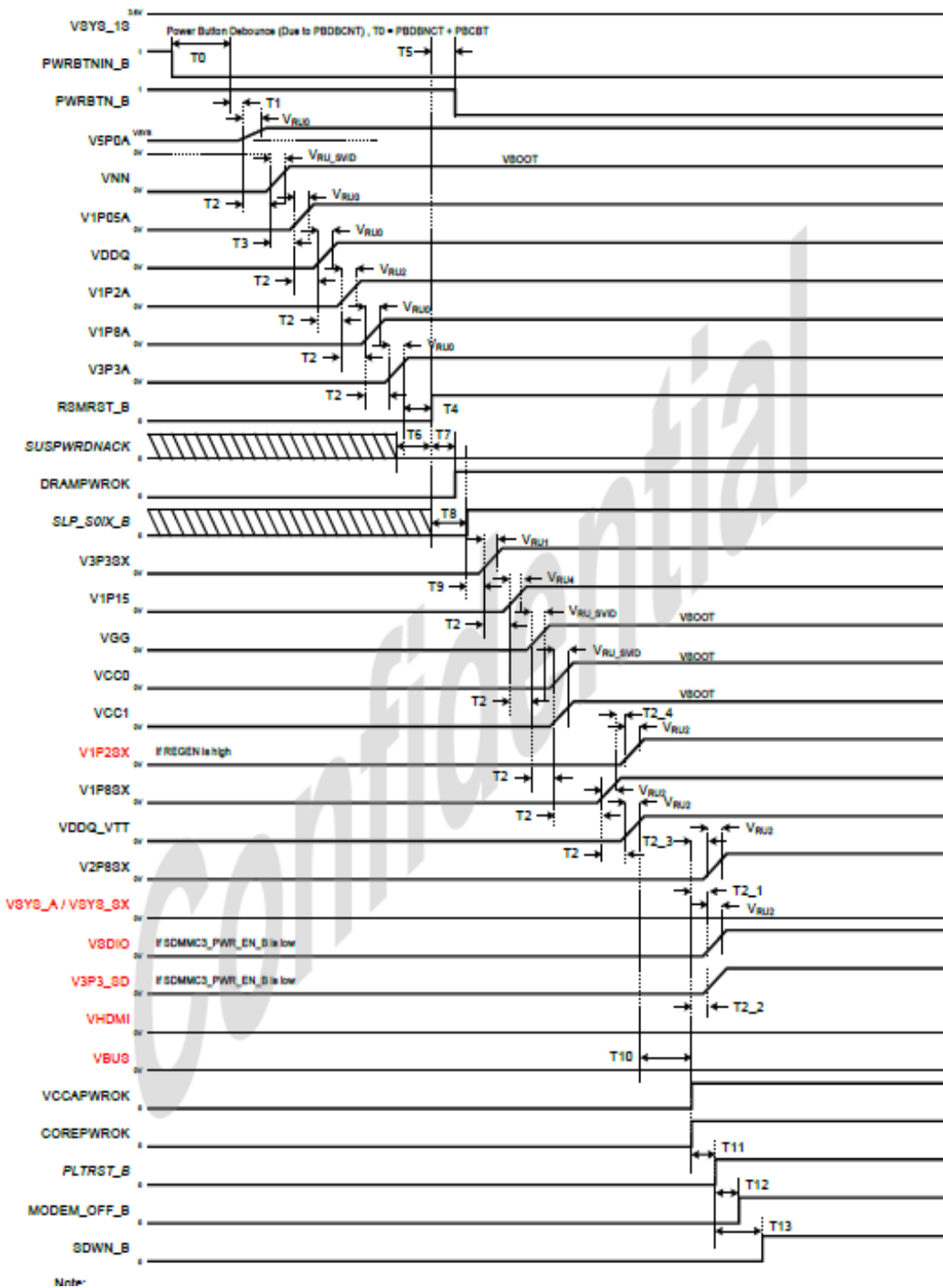
Sheet 61 of 73

SOC Cherry Trail POWERMAP



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Parameter	Description	Min.	Typ.	Max.	Unit
T0	Power Button Debounce Time (Due to PBDBNCT register)	PBDBNCT -10%	PBDBNCT	PBDBNCT +10%	ms
T1	After battery detect or power button debounce time to VSP0A turn on delay	0	24	500	µs
T2	Rail to subsequent rail turn-on delay for all rails unless specified otherwise	0.01	1	2	ms
T2_1	COREPWROK assertion (high) to VSDIO turn on (10%) delay	10	50	100	µs
T2_2	COREPWROK assertion (high) to V3P3_SD turn on (10%) delay	0.1	0.45	1	ms
T2_3	COREPWROK assertion (high) to V2P8SX turn on (10%) delay	0	10	50	µs
T2_4	V1P8SX Valid (90%) to V1P2SX turn on (10%) delay	0	30	60	µs
T3	VNN to V1P05A turn on delay (CCB 034 from Intel)	0.5	1	2	ms
T4	V3P3A valid (90% level) to RSMRST_B de-assertion (high) if SUSPWRDNACK is low	0	24	500	µs
T5	RSMRST_B de-assertion (high) to the instant when the BD2613GW outputs a level shifted copy of PWRBTN_B, i.e. PWRBTN_B	0	24	32	µs
T6	SUSPWRDNACK de-assertion (low) to RSMRST_B de-assertion (high)	0	-	-	µs
T7	RSMRST_B de-assertion (low) to DRAMPWROK assertion (high)	0	24	32	µs
T8	RSMRST_B de-assertion (high) to SLP_S0IX_B de-assertion (high)	20	-	-	µs
T9	SLP_S0IX_B de-assertion (high) to V3P3SX start to turn on (10% output voltage level) delay	0	250	500	µs
T10	Core rails valid to VCCAPWROK and COREPWROK assertion (high)	DTPWROK -20%	DTPWROK	DTPWROK +20%	ms
T11	COREPWROK assertion (high) to PLTRST_B de-assertion (high)	60	-	-	µs
T12	MODEM_OFF_B de-assertion (high) delay from PLTRST_B de-assertion (high)	10	20	40	µs
T13	SDWN_B de-assertion (high) delay from PLTRST_B de-assertion (high)	40	60	75	µs

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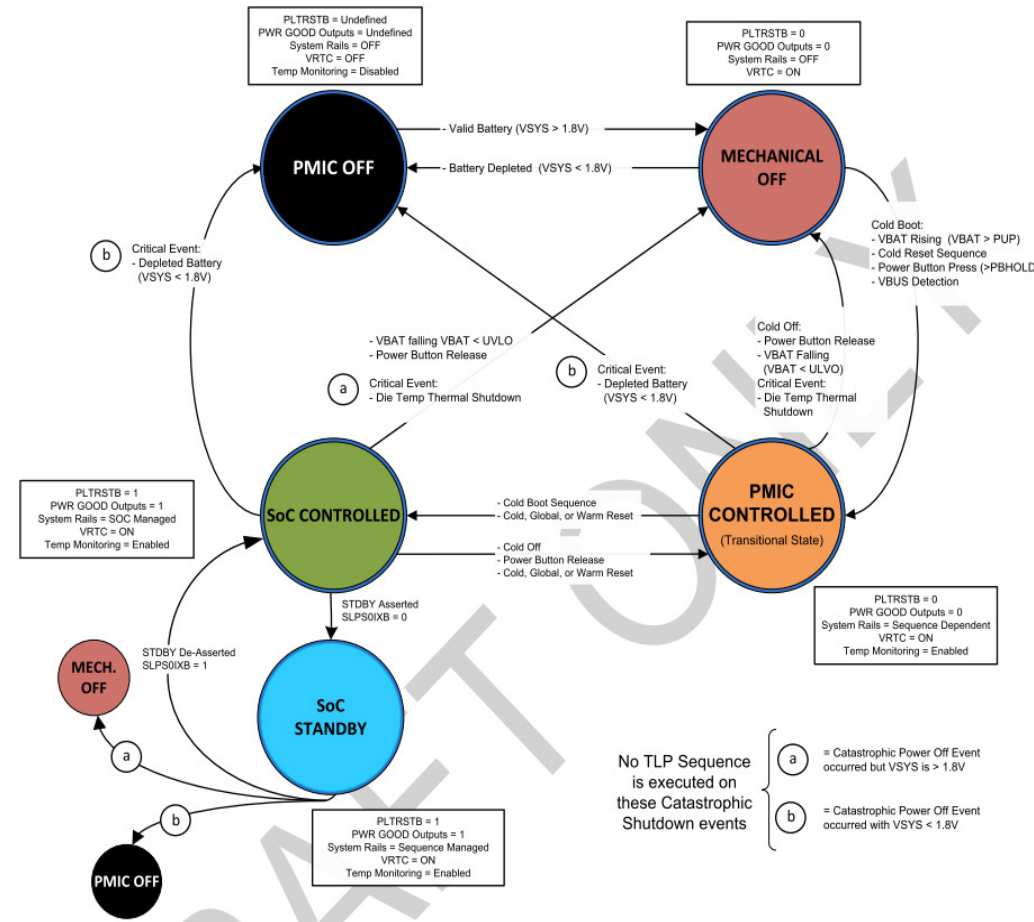
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Title **64_Power Sequence Timing**

Size Document Number **Blackwell T4** Rev **-1**

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	PART	BUCK1	BUCK2	BUCK3	BUCK4	BUCK5	BUCK6	LD01	LD02	LD03	VRTC LD04	VREFDQ LD05	LD06	LD07	LD08	LD09	LD010	LD011	LD012	LD013	LD014	Comment	
PMIC OFF	BYT	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	CHT	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
Mechanical Off	BYT	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
	CHT	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
SoC Controlled	BYT	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	Disabled by default. SoC can enable/disable according to system activity								VREFT can be turned on and off for thermistor and GPADC biasing	
	CHT	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	Disabled by default. SoC can enable/disable according to system activity									
SoC Stand-by	BYT	OFF	OFF	ON	V _{SLP}	ON	V _{SLP}	ON	OFF	ON	ON	ON	ON	Will keep whatever state had before entering standby								I2C is operational VREFT can be turned on and off for thermistor and GPADC biasing	
	CHT	OFF	ON	V _{SLP}	V _{SLP}	ON	OFF	ON	ON	ON	ON	ON	ON	Will keep whatever state had before entering standby									

LDO7-LDO14 will keep whatever state before entering standby, it's up to the user whether to enable/disable. State machine won't enforce the behavior in this case.

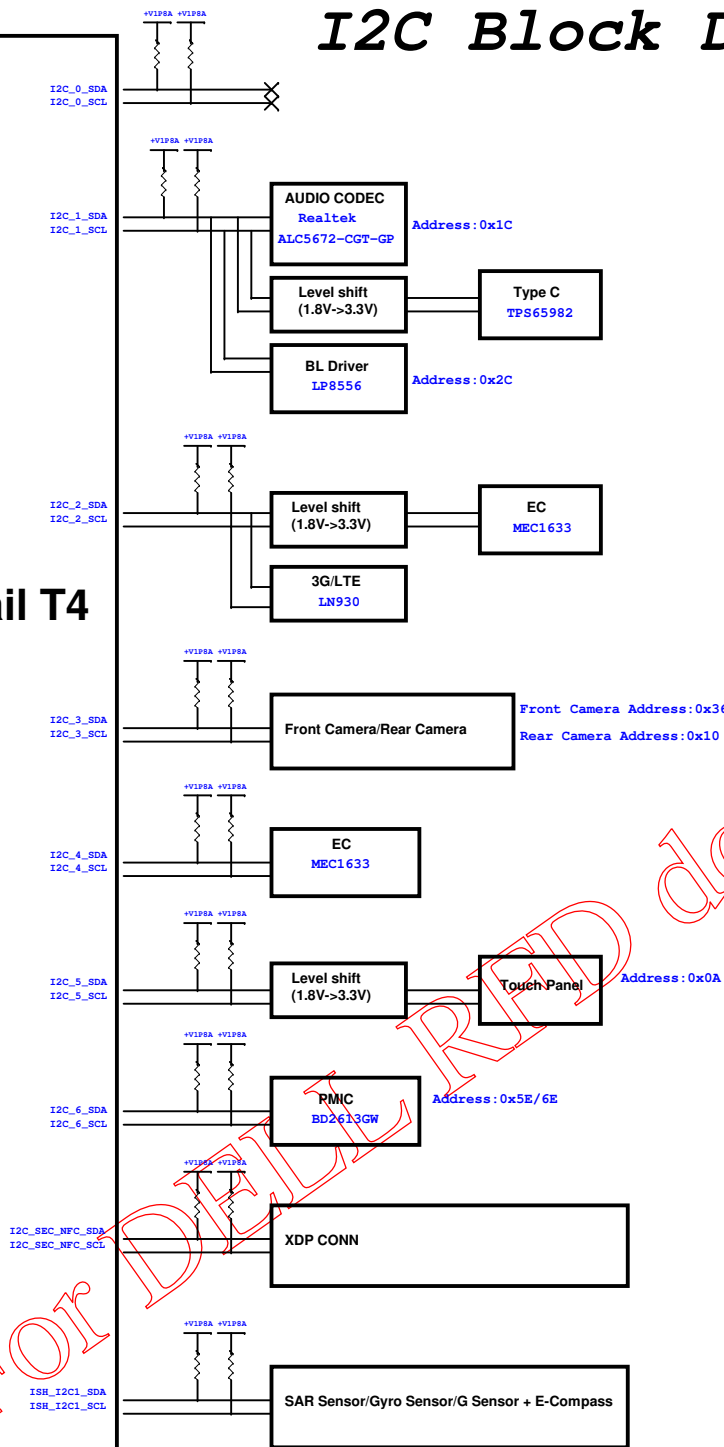
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Title	65_Power State
Size	Document Number Blackwell T4
Date	Thursday, October 01, 2015
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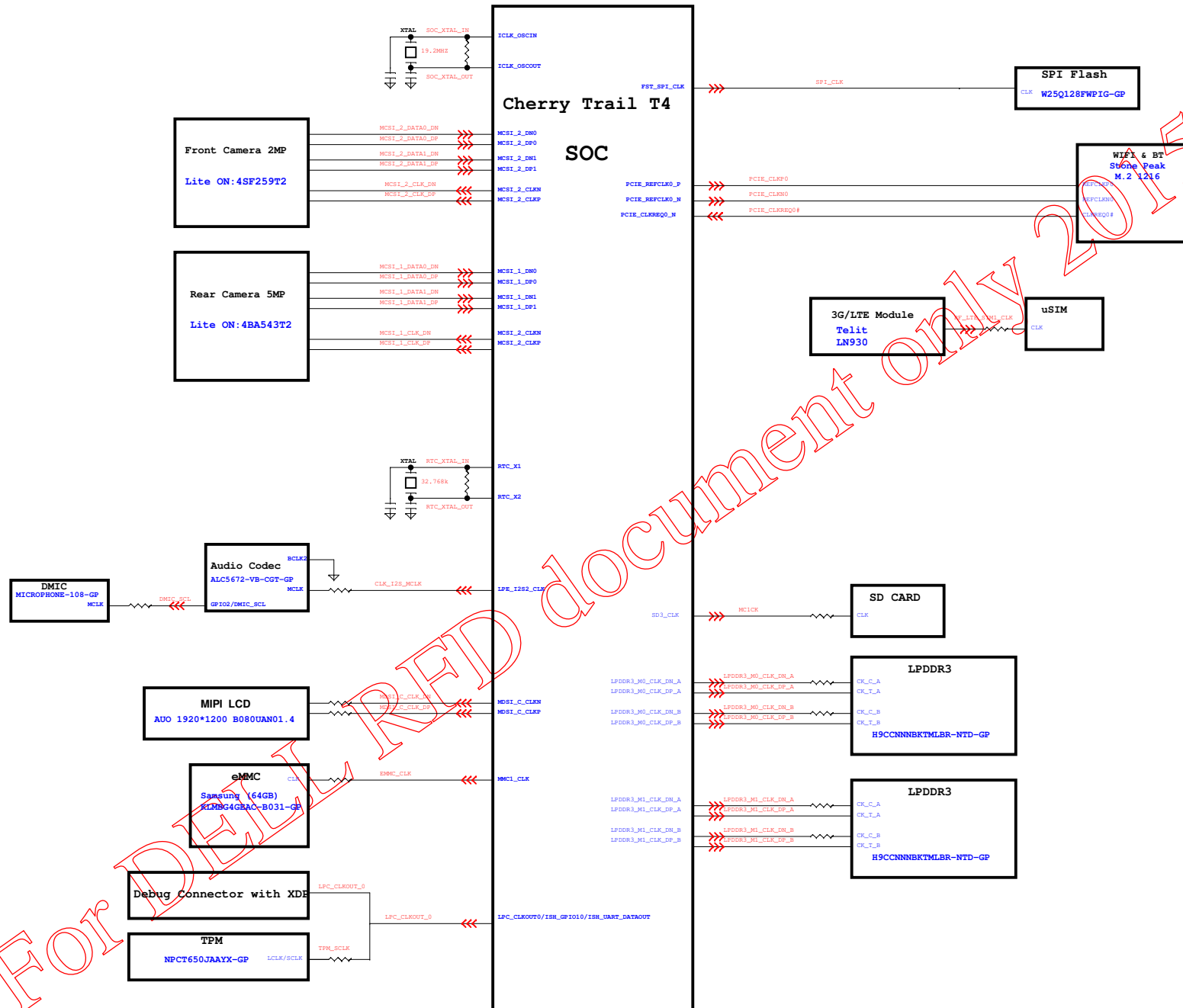
I2C Block Diagram

Intel Cherry Trail T4



Device	Blackwell-T3	Blackwell-T4	Somerset-T4
CODEC	I2C1	I2C1	I2C1
AMP	---	---	I2C1
Type C PD controller	I2C1/EC I2C7	I2C1/EC_I2C7	I2C1/EC_I2C7
3G/LTE	I2C1	I2C2	I2C2
EC (I2C_0)	I2C2	I2C2	I2C2
Front CAMERA	I2C2	I2C3	I2C3
Rear CAMERA	I2C2	I2C3	I2C3
ISP	I2C2	I2C3	I2C3
uHDMI	---	---	DDIO_DDC
NFC	I2C2	NFC_I2C	NFC_I2C
EC (I2C_5)	I2C4	I2C4	I2C4
LCD Backlight Driver	I2C1	I2C1	---
Touch	I2C5	I2C5	I2C5
PMIC	I2C6	I2C6	I2C6
A+Gyro sensor/ Gyro sensor	ISH_I2C	ISH_I2C	ISH_I2C
E sensor/ E+A sensor	ISH_I2C	ISH_I2C	ISH_I2C
Sar Sensor	ISH_I2C	ISH_I2C	ISH_I2C
Battery	EC_SMB3	EC_SMB3	EC_SMB3
Charger	EC_I2C4	EC_I2C4	EC_I2C4

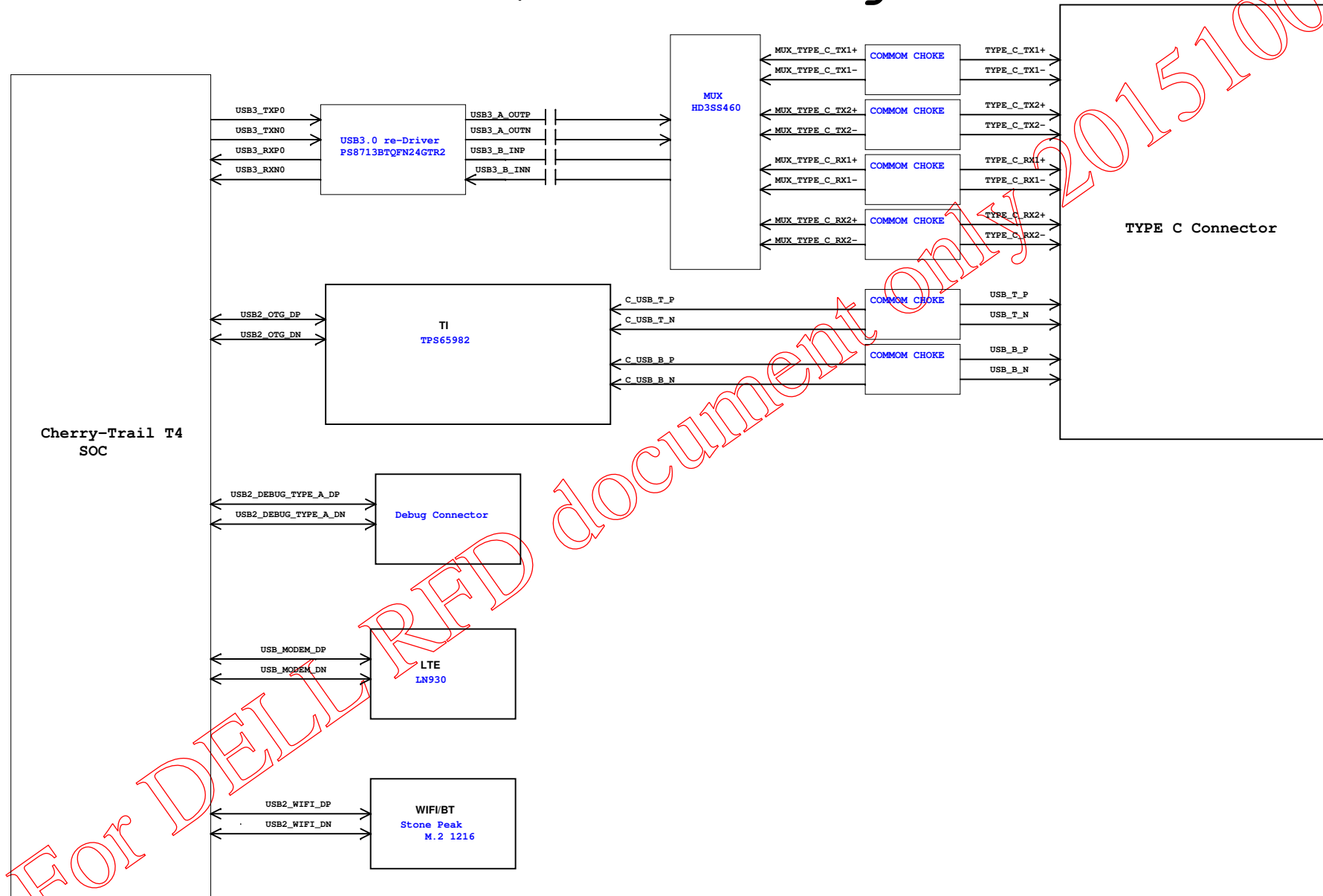
CLOCK Block Diagram



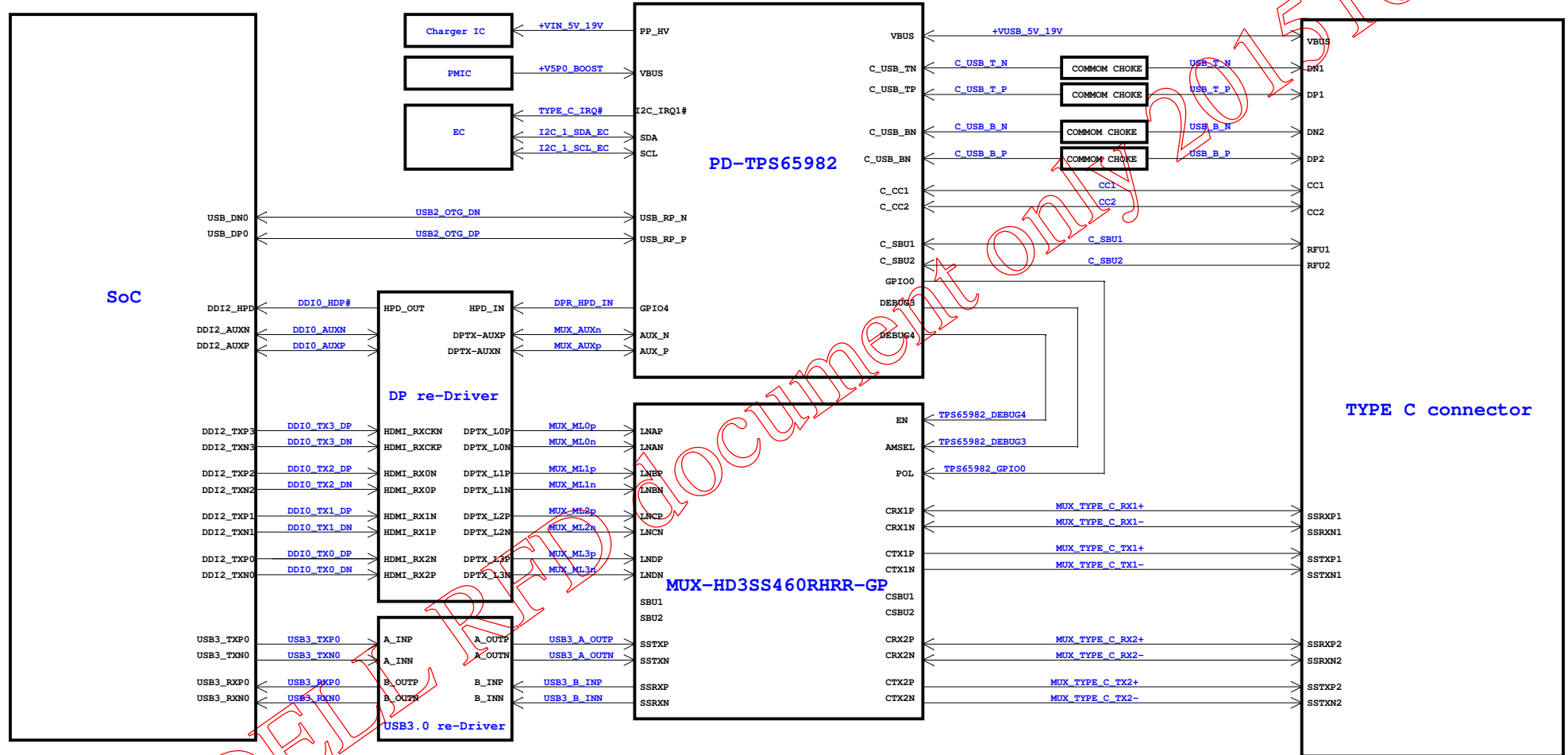
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For		67_CLK BLOCK DIAGRAM	
Doc	Doc Number	Rev	Rev
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Date	2015.05.10	Rev	1

USB I/O Block Diagram



TYPE C Block Diagram



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Title **70_TYPE C BLOCK DIAGRAM(2/2)(Reserved)**

Size	Document Number Blackwell T4	Rev -1
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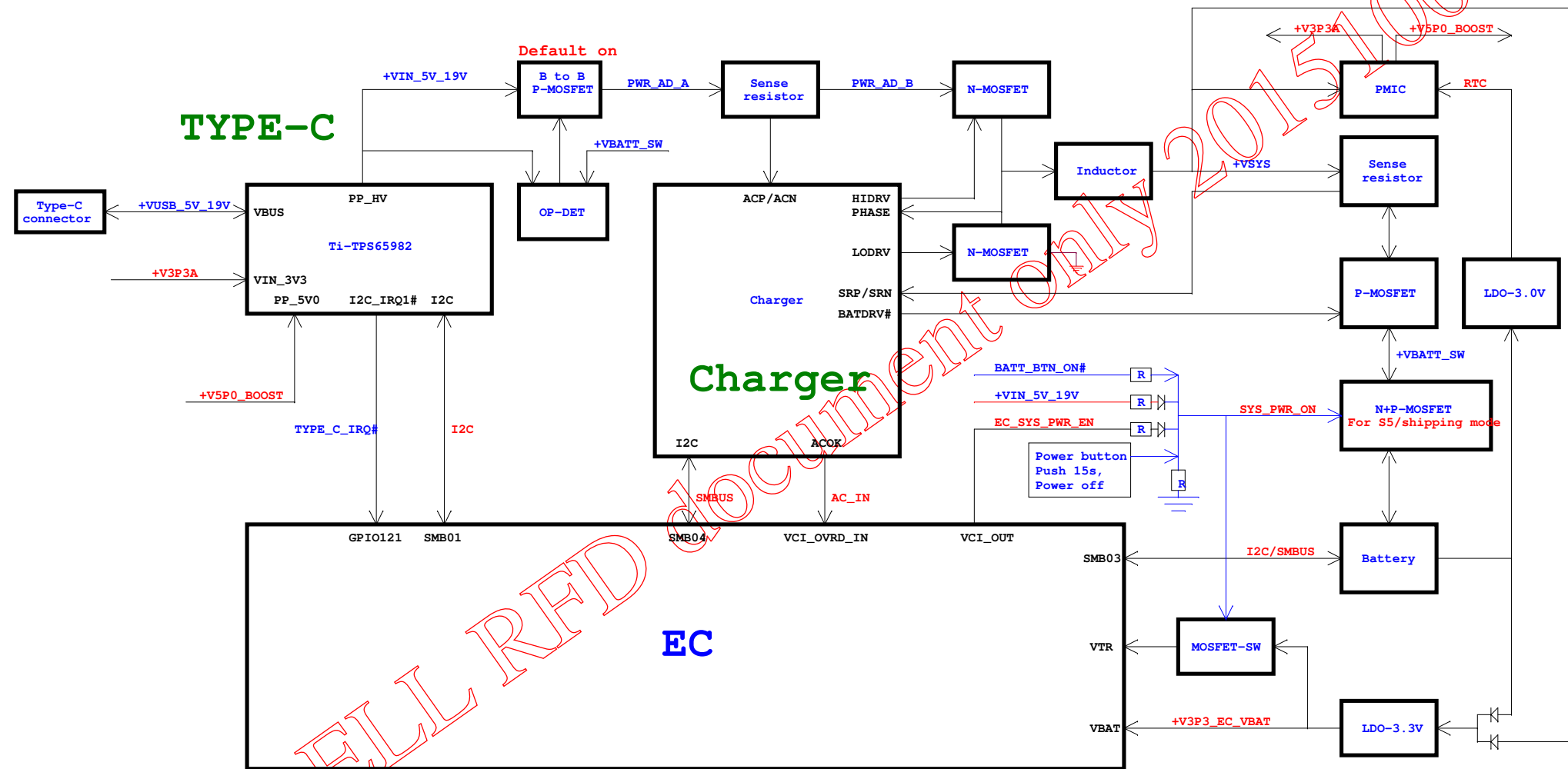
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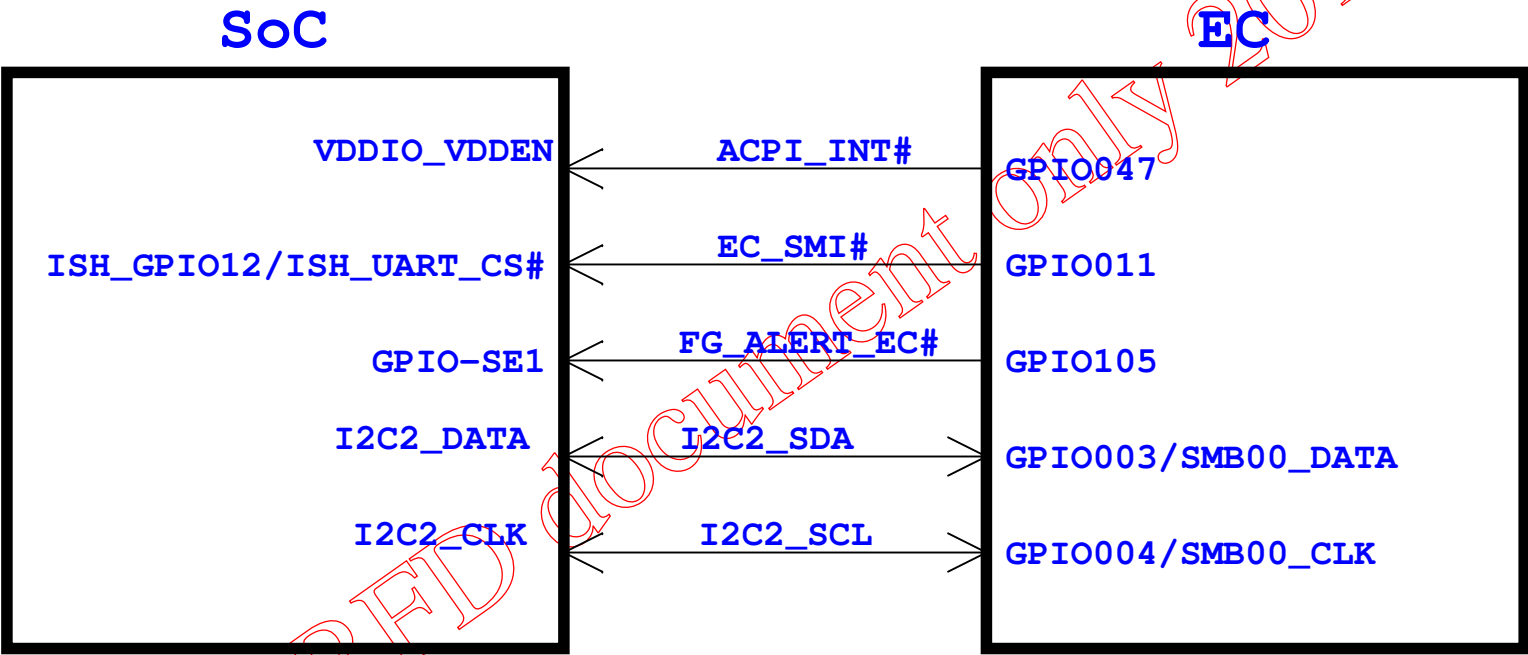
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Title					
71_Change History					
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Power block diagram



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EC/SoC interface



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Title **73_EC/SoC interface**

Size Document Number
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